AD A047110

RADC-TR-77-321
Final Technical Report
October 1977

THERMAL RESISTANCE OF MICROELECTRONIC PACKAGES

General Electric Company

DDC
RECEIVED
DEC 1 1977
F

Approved for public release; distribution unlimited.

AD No.
DDC FILE COPY

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

This report has been reviewed and is approved for publication.

APPROVED: Regis C. Hilow

REGIS C. HILOW
Project Engineer

APPROVED: Joseph J. Naresky

JOSEPH J. NARESKY
Chief, Reliability and Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRM) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: RADC-TR-77-321	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): THERMAL RESISTANCE OF MICROELECTRONIC PACKAGES		5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report. 6 April 1976 - 6 May 1977
		6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): James W. Analow, Gene K. Baxter, J. Walter Brouillette		8. CONTRACT OR GRANT NUMBER(s): F30602-76-C-0228
9. PERFORMING ORGANIZATION NAME AND ADDRESS: General Electric Company, Electronics Laboratory, Syracuse NY 13221		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F 23380101
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRM), Griffiss AFB NY 13441		12. REPORT DATE: October 1977
		13. NUMBER OF PAGES: 96
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same		15. SECURITY CLASS. (of this report): UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Regis C. Hilow (RBRM)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Integrated Circuits, Junction Temperature, Chip-Carrier Temperature, Computer Simulation, Experimental Testing, Thermal Resistance, Wire-Bonding, Junction Size, Elevated Temperature, Infrared Temperature Measurement, Thermal Time Constant, Temperature Response, Thermal Models, Experimental Data, Microelectronic Packages

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Computer simulation, IR and electrical temperature measurements were compared and evaluated for special thermal test packages. The junction size was varied and elevated chip-carrier temperatures were studied to determine their effects on the thermal characteristics. In addition a comparison of the film-carrier chip interconnection technique versus wire-bonding techniques was made. In general, the data showed that thermal resistance increased significantly with elevated temperatures and with decreasing junction size. Thermal time →

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

149 508

constants increased with elevated temperature and increasing junction size. Little difference was found between the film carrier and wire-bond interconnection techniques when the chip is bonded to a chip-carrier, but the film carrier is significantly better if the chip is heat sunk only through its leads.

ACKNOWLEDGEMENTS

We would like to acknowledge the help we have received during this project by expressing our sincere thanks to Mr. Ray Triche and Mr. Alex Louie who performed the experimental tests, to Mr. Edwin Fung who helped with the Computer Simulations, and to Mr. Vladimir Popoff and his staff who prepared the manuscript.

We would also like to express our special thanks to Mr. Regis C. Hilow, RADC Project Engineer, for his cooperation and interest through this project.

This project was sponsored by the USAF/Rome Air Development Center (RBRM), Griffiss AFB, Rome, N.Y., 13441 under Contract No. F30602-76-C-0228, Purchase Request No. N-6-5011 (GE/Electronics Laboratory Project No. 260-DZ-894400).

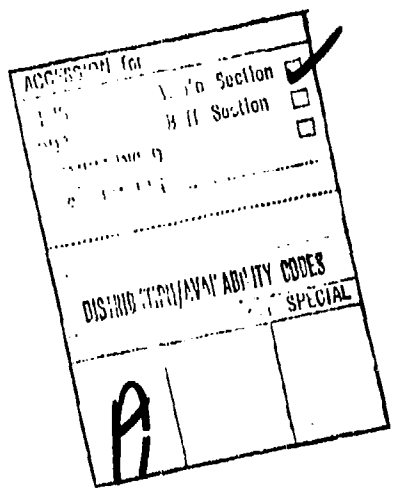


TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont.)

LIST OF TABLES

GLOSSARY OF TERMS

A	Area ($inch^2$)
D	Diameter (inch)
$\dot{q}$	Power Input (watts)
T	Temperature (^oC)
Θ	Thermal Resistance ($^oC/W$)
τ	Thermal Time Constant (μsec and msec)

SUBSCRIPTS

JA	Junction Average
JR	Junction Region
JP	Junction Peak
SA	Surface Average
CC	Chip Carrier
J	Junction
C	Chip
HS	Heat Sink
M	Model
e	equivalent
L	lead
CR	Connection Region
X, Y	Generic Location
SS	Steady State
S	Surface

EVALUATION

The objective of this effort was to determine the thermal characteristics of special microelectronic devices, such as beam lead and film carrier type packages and small geometry type transistors used in complex microcircuits. Also, the thermal characteristic of JAN type microcircuits were evaluated at accelerated temperatures. This effort was a continuation of an initial study aimed at refining the test procedures of Method 1012 of MIL-STD-883 for measuring thermal resistance and thermal time constants of microelectronic devices.

The approach that was taken to satisfy the above objectives was, as in the initial contract, to pursue a balanced program consisting of computer-aided simulation and experimental testing. Detail results of the three major tasks, small junction temperature characterization, high temperature thermal characterization and film carrier thermal characterization are contained in this report. Significant results are as follows:

a. Film carrier devices are thermally inferior to conventional devices unless their die is attached to the substrate.

b. Present infrared measurement techniques are limited in measuring small junction devices.

c. Thermal time constant varies with the junction area to the 0.45 power.

d. Thermal resistance varies with high temperatures mainly due to the change in the thermal conductivity of silicon. Temperature, not power, causes these variations.

e. Thermal models for film carrier and beam lead devices were developed.

This effort concludes the two-year evaluation of the thermal characteristics of microelectronic packages and the state-of-the-art thermal measurement techniques. The results of this effort and the past effort will be used to revise Method 1012 of MIL-STD-883 and to correct present values of thermal resistance contained in M38510 detail specification.

Roger C. Hilow

REGIS C. HILOW
Project Engineer

1.0 INTRODUCTION

1.1 PREVIOUS STUDY

This report describes the result of a continuing study of thermal characteristics and measurement techniques for microelectronic packages. The previous study, "Thermal Resistance of Microelectronic Packages," was performed in 1974-75 under the sponsorship of the USAF Systems Command/Rome Air Development Center, Griffiss AFB, Rome, New York [. That work was concerned, primarily, with an evaluation of the accuracy of thermal measurement techniques and as a result of that study, new recommended methods for measuring the thermal characteristics of microelectronic packages were developed and a proposed revision of method 1012 (Thermal Characteristics) of MIL-STD-883 (Test Methods and Procedures for Microelectronics) was written [2]. Summaries from these two references are included as Appendices A and B.

1.2 SUMMARY OF 1976-77 PROJECT

The purpose of this project was to further define the thermal charac teristics of microelectronics packages. It was divided into three tasks:

1. Junction Temperature Characterization

To assess and refine thermal measurement methods for the determination of Junction Peak, Junction Average and Junction Region Temperature of small junction transistors (area < 6.25 mil^2) in state-of-the-art microcircuits.

2. High Temperature Thermal Characterization

To determine thermal characteristics of microelectronic packages operating at elevated Chip Carrier Temperature ($175^{\circ}C < T_{CC} < 250^{\circ}C$),

3. Film Carrier Interconnection Thermal Characterization

To detemine the effects of Film Carrier Leads on the thermal characteristics of microelectronic chips and packages.

A balanced program, consisting of computer-aided simulation and experimental testing, was used to achieve the above-listed objectives.

The basic test vehicle for both the simulations and experimental testing was a special thermal test chip, SCP 14, which has 32 independently accessible transistor Junctions located in 16 pairs on the chip [3]. Figure 1.1 is a photograph of this chip. For experimental use, the chip is over-glassed and eutectically bonded to a gold metallized alumina substrate. The four center-most junctions are normally powered during testing. The basic test setup with Infrared Microscope is shown in Figure 1.2. A chip mounted in a 40 pin dual-in-line (DIL) ceramic package, is shown in the Figure. The complete test setup for each task is described in the appropriate sections of this report.

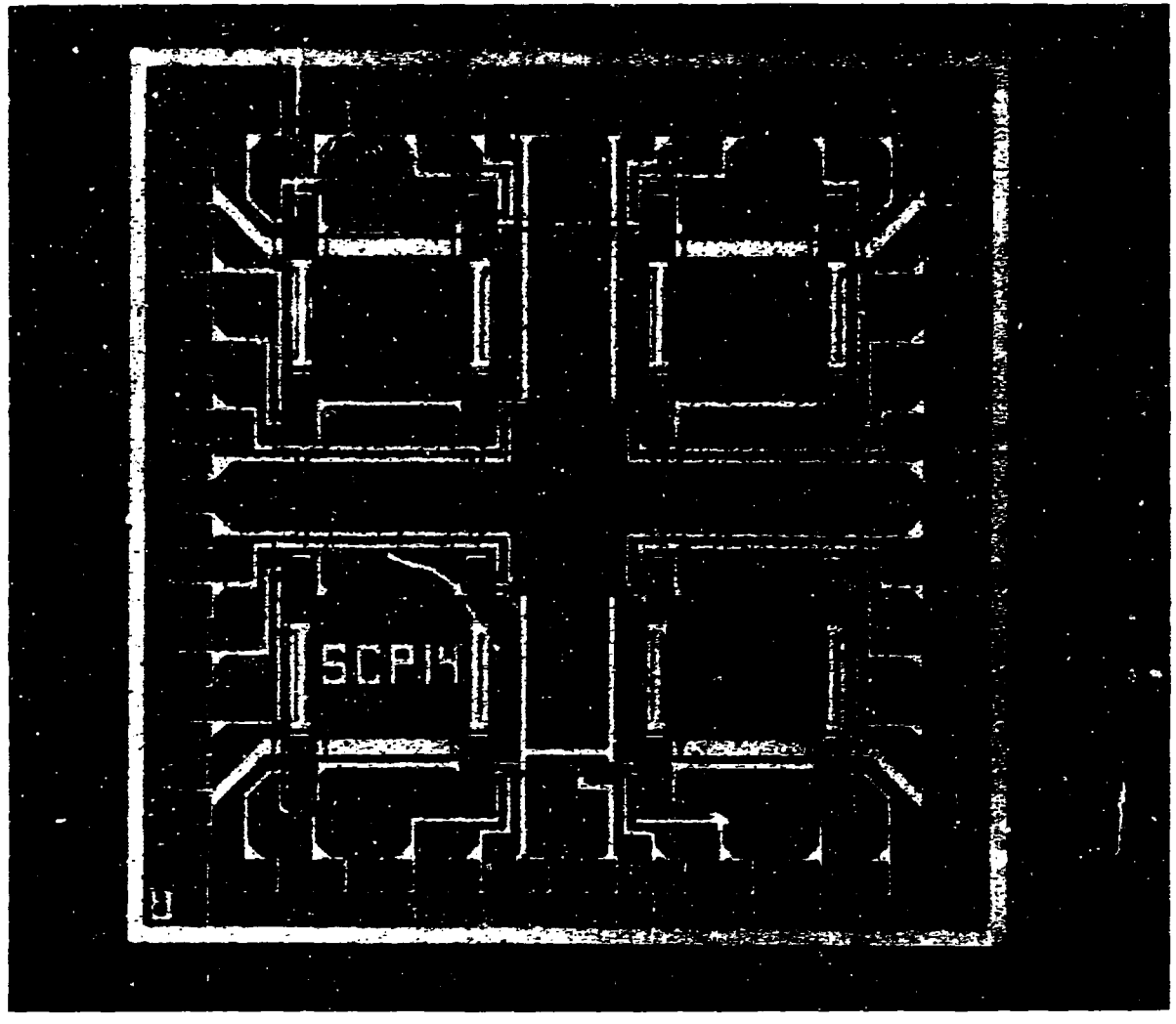


Figure 1.1. Thermal Test Chip

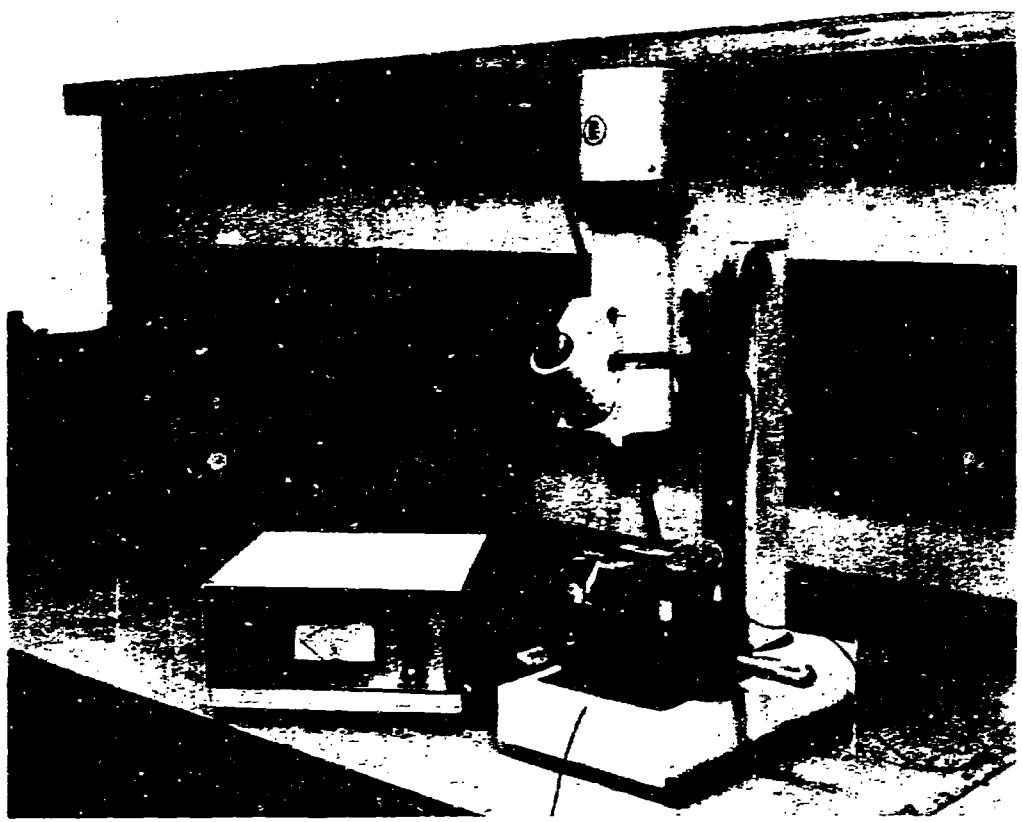


Figure 1.2 Basic Infrared Microscope Set-up

1.3 COMPUTER PROGRAM

The computer program for the thermal simulations is entitled THTD (Transient Heat Transfer - Version D). This program is a general purpose heat transfer program capable of handling a wide variety of complicated problems. The program was written initially in 1958 and since then has undergone many improvements that have made it a reliable code. It is currently in use by numerous departments within the General Electric Company.

There are many special features of THTD. It can handle, for example, transient and steady-state problems involving complex three-dimensional geometry, multiple materials and boundary conditions, internal heat generation, surface flux, external and internal radiation, fluid flow, material phase change, temperature-dependent material properties and time-dependent boundary conditions.

The THTD program uses finite difference techniques, in which the physical configuration of a problem is first divided into many small geometrical volumes called nodes. Each node has an associated thermal heat-balance equation that relates the temperature, material properties and geometry of the node to similar properties of the adjacent nodes or prescribed boundary conditions. A set of N nodes yields a system of N simultaneous equations, which are solved using a numerical iterative technique based on the "Gauss-Seidel" algorithm. Special temperature and heat balance convergence criteria is monitored by the program to insure that a complete and accurate solution has been attained. Specific temperature data are, thus, obtained for specially selected inputs. From these data the thermal characteristics of the device can be determined via engineering judgment and interpretation. The important thing is that the computed solution provides data that are consistent with all prescribed boundary conditions, material properties, complex geometries, etc. Experience with this method of simulation has consistently yielded results that are in good agreement when compared with reliable experimental measurements.

1.4 MATHEMATICAL MODELS

In order to provide numerical input data for the computer program, mathematical models are first developed. An accurate model of a complex physical device, such as the integrated circuit, requires a great number of nodal descriptions. To simplify the problem, superposition techniques are generally used. In this study two models were developed; one to simulate the junction region in the chip, and a second to simulate the chip and chip carrier (substrate) configuration.

The chip model, shown in Figure 1.3 was developed to determine the general chip and substrate, i.e. chip-carrier, thermal characteristics. The representative thermal resistance values shown in Figure 1.3 are taken with respect to a thermal probe, which is shown in contact with the bottom of the substrate. The thermal probe is used in experiments to determine the chip carrier temperature. Since the probe is generally at a higher temperature than the outer portions of the substrate, this produces the negative resistance

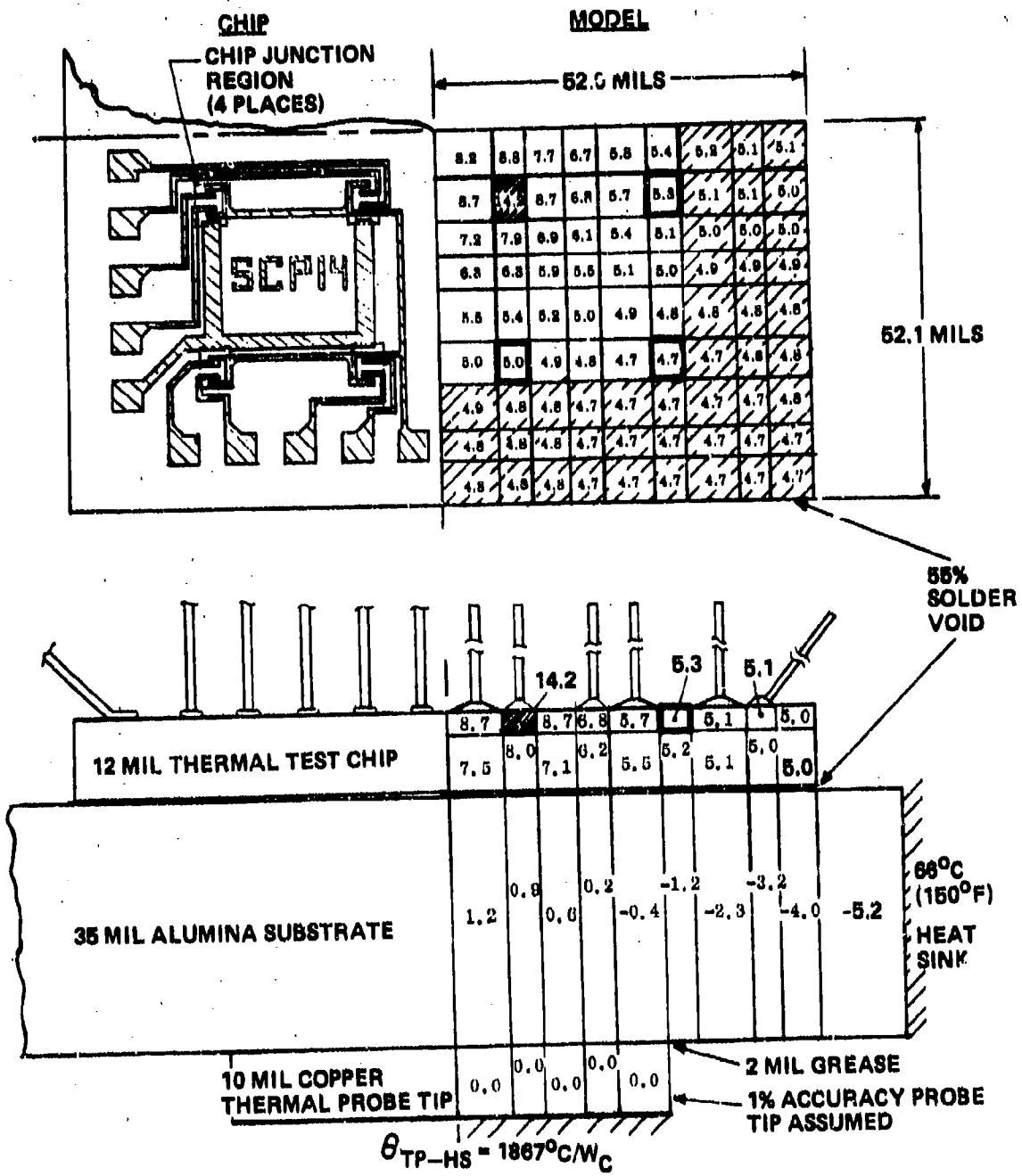


Figure 1.3 SCP-14 Chip Mathematical Model

values shown in the figure. For this study the thermal probe was not simulated in the model. Instead, the thermal data will be shown with respect to the chip carrier, defined here as that volume of the substrate located directly below the chip. The chip model consisted of 287 nodes and represents one quadrant of the chip and chip carrier. The silicon chip is 12 mils thick, has 40 aluminum wire leads attached, and has a half-mil AuSi eutectic bonded to a 35 mil thick alumina substrate. Power dissipation for this model is simulated as a uniform volumetric heat generation in the area designated as the chip junction region.

A model of the junction region was also developed to determine the specific characteristics near each pair of junctions on the chip. The physical details of this region are shown in Figure 1.4 and the mathematical model of the junction region is shown in Figure 1.5. The model consists of 467 nodes, divided into six layers, to simulate the geometry and characteristics of the aluminum metallization, the silicon dioxide glassivation and the bulk silicon of the chip near the junction. Power dissipation was simulated, in this model, by uniform volumetric heat generation in a finite volume of the emitter-base transistor junction as shown in Figures 1.4 and 1.5.

To study thermal effects in an electronic device, the computer program must be able to handle temperature-dependent material properties. In the simulations discussed here, specific heat and thermal conductivity, obtained from references [4] and [5], were input for the models. The variation of thermal conductivity for silicon and alumina, for example, is shown in Figure 1.6. These curves show that there is a significant variation in thermal conductivity for both the substrate and the chip. That variation depends on the absolute temperature of the material. Since the temperature distribution within the chip and chip carrier can vary considerably, the thermal conductivity can also vary considerably depending on location within the chip and the chip carrier.

1.5 TECHNICAL APPROACH

The overall thermal characteristics of the chip and junction have been determined by superimposing the thermal simulation data from the junction model onto that of the chip model. The superposition procedure is, thus, to first predict the rise in average junction region temperature (T_{JR}) relative to that of the chip carrier temperature (T_{CC}), by using the chip model. Then the junction region model is used to predict the rise in junction peak and average temperature (T_{JP} and T_{JA}, respectively) relative to that of the average junction region temperature. The chip carrier temperature is defined as the average temperature of that volume of the alumina substrate directly under the chip. The junction region is that volume represented by solid cross-hatching in Figure 1.[illegible]. The single-node junction region temperature obtained from the chip model, is equal to the average temperature of all nodes in the whole junction region model. The boundary conditions of the junction region model are adjusted to ensure that this occurs. This matching of temperatures is necessary to ensure that temperature-dependent material properties are automatically included in the temperature response characteristics. From this superposition then, an accurate value of the junction peak temperature (T_{JP}) and the junction average temperature (T_{JA}) are found for any given chip carrier temperature. The junction peak temperature is the highest

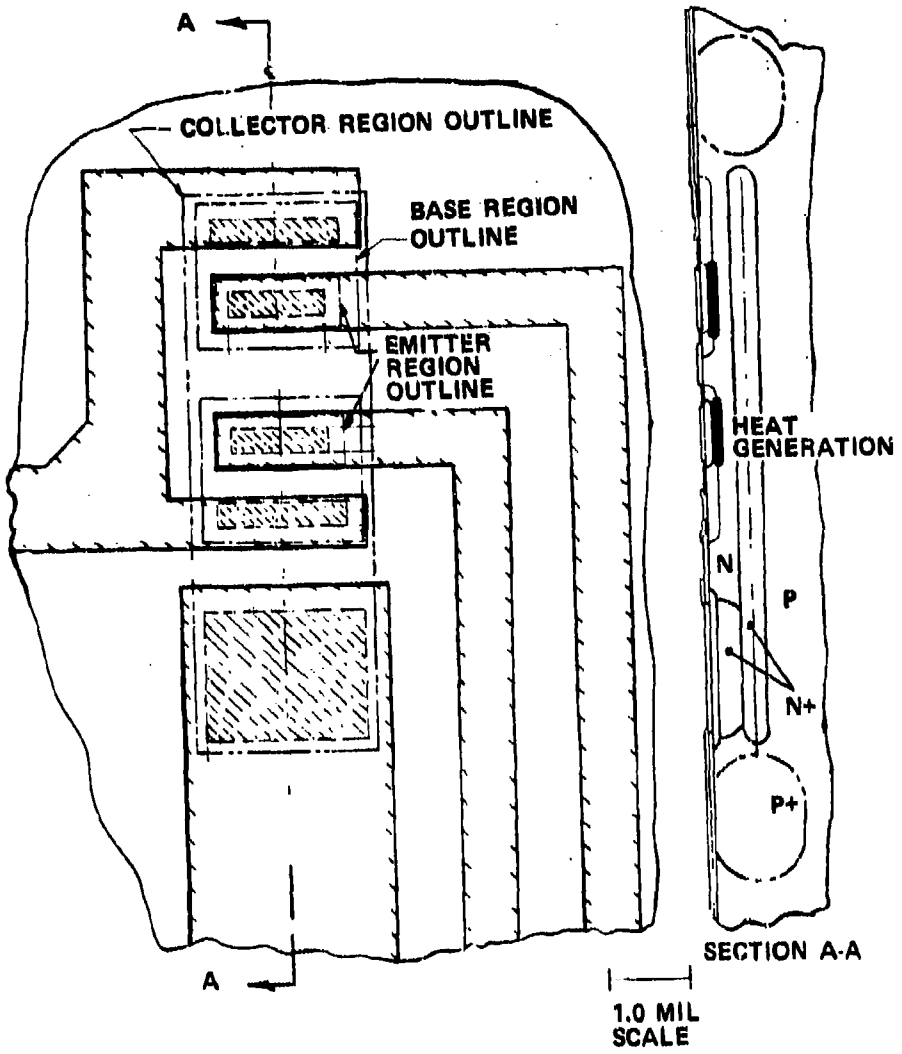


Figure 1.4 Physical Characteristics of the Junction Region of Thermal Test Chip

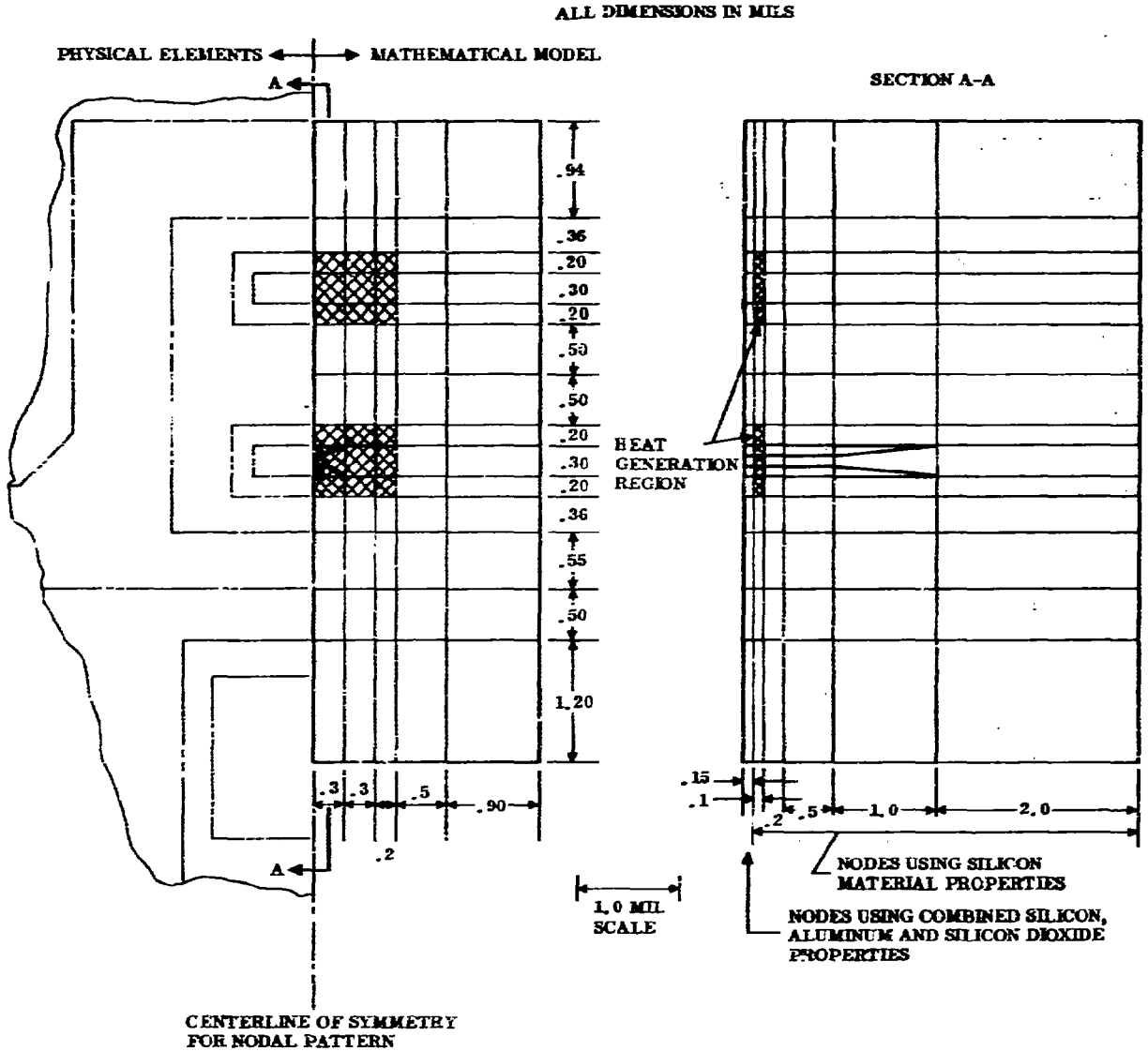


Figure 1.5 SCP 14 Junction Region Mathematical Model

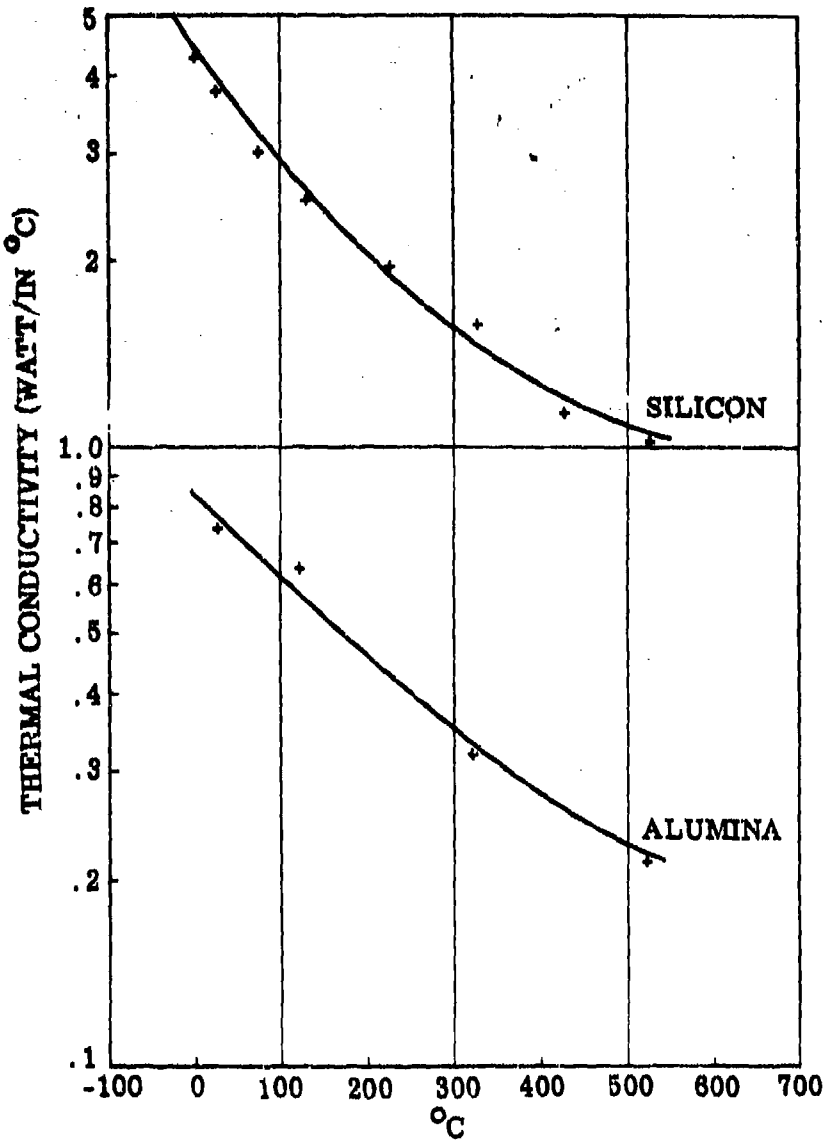


Figure 1.6 Effect of Temperature on Thermal Conductivity of Silicon and Alumina

temperature within the heat generation volume of the junction region model (see Figure 1.5) and the junction average temperature is the average temperature of that volume. Having found these temperatures, the thermal resistance, relative to some parameter, say, the chip carrier -- namely, θ_{JP-CC}, θ_{JA-CC} and θ_{JR-CC} -- can be determined from

$$\theta_{XX-CC} = \frac{T_{XX} - T_{CC}}{\dot{q}_C} ,$$

where $\dot{q}_C$ is the power dissipation in the chip.

The values of the thermal time constants, τ_{JP-CC}, τ_{JA-CC}, and τ_{JR-CC}, are determined in a similar manner using superimposed transient computer simulation. The thermal time constant is defined here as the time required for the temperature rise, relative to the chip carrier temperature, to reach 63.2% of its final steady state value after a step function in power dissipation is applied.

2.0 JUNCTION TEMPERATURE CHARACTERISTICS

2.1 COMPUTER-AIDED SIMULATION AND ANALYSIS

2.1.1 General Remarks

The purpose of the simulations in this portion of the study is to show the effect of different-sized junction areas on the thermal characteristics of the microcircuit.

To accomplish this the chip model (Figure 1.3) was used to predict the Junction Region Temperature (T_{JR}); then the junction region model, (shown in Figure 1.5), was modified so that it could be used to simulate various-sized junction power dissipation areas (A_J). These areas ranged from 0.18 $mils^2$ to 10.9 $mils^2$; Figure 2.1 depicts the range of areas used and the silicon layer in which the power dissipation was simulated.

Simulations were then made to determine Junction Peak Temperature (T_{JP}), Junction Average Temperature (T_{JA}), and Surface Average Temperature (T_{SA}) for the range of junction areas. For each junction area, the thermal time constants and thermal resistance values were computed. The variation of thermal resistance with chip-carrier temperature (T_{CC}) and power dissipation rate ($\dot{q}_C$) were also computed for the selected junction areas.

2.1.2 Thermal Characteristics

2.1.2.1 Thermal Resistance Values of the Various-Sized Junction Areas

The thermal resistance for the various-sized Junction areas are summarized in Table 2.1. These were calculated from the computer simulated temperatures for T_{JR}, T_{JP}, AND T_{JA}, with T_{CC} = 60°C and $\dot{q}_C$ = 1.5 watts for each area, using the relationship $\theta_{XX-YY} = \frac{T_{XX} - T_{YY}}{\dot{q}_C}$. These thermal resistance values were then used to plot the data shown in Figure 2.2, which shows that the values of Thermal Resistance, θ_{JP-CC}, and θ_{JA-CC}, decrease exponentially as a function of increasing junction size (A_J).

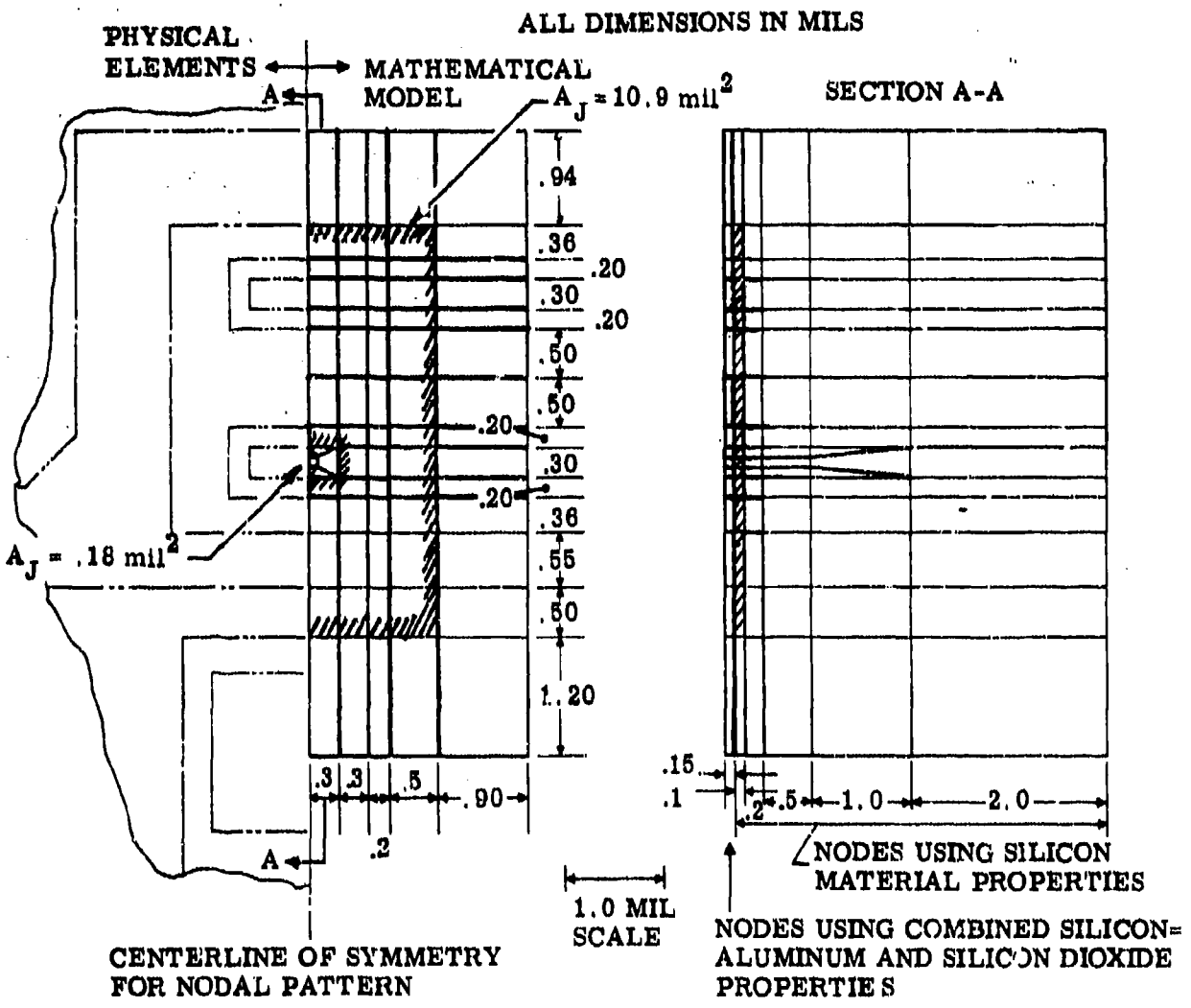


Figure 2.1 Nodal Pattern for Model of Thermal Chip Junction Region (SCP-14 Chip) Showing Range of A_J Used

TABLE 2.1

COMPARISON OF THERMAL RESISTANCE VALUES ($^{o}C/W_C$) FOR VARIOUS SIZED JUNCTION AREAS WITH CHIP CARRIER TEMPERATURE (T_{CC}) OF 60°C AND CHIP POWER ($\dot{q}_C$) OF 1.5 WATTS

AREA (MIL^2)	θ_{JP-JR}	θ_{JA-JR}	θ_{JR-CC}	θ_{JP-CC}	θ_{JA-CC}
.18	82.4	73.0	10.5	92.9	83.5
.30	68.3	62.1	↕	78.8	72.6
.84	39.4	34.1	↕	49.9	44.6
1.12	33.1	28.2	↕	43.6	38.7
4.05	15.8	13.0	↕	26.3	23.5
6.86	11.6	9.2	↕	22.1	19.7
10.92	8.0	6.1	10.5	18.5	16.6

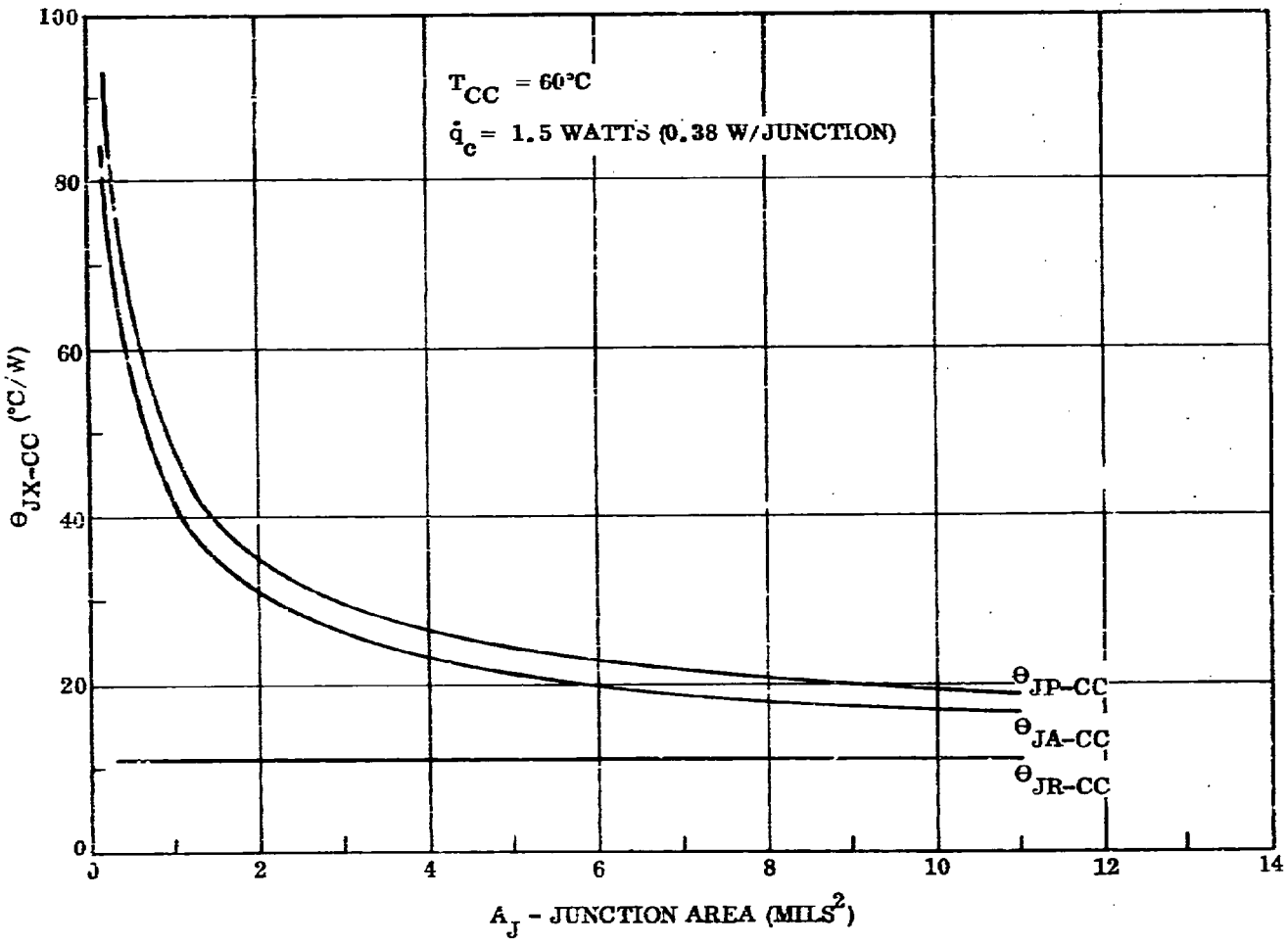


Figure 2.2 Comparison of Thermal Resistance Values as a Function of Junction Size

2.1.2.2 Temperature Distribution and Surface Temperature

To obtain an idea of the temperature distribution within the junction region of a microelectronics package, isothermal plots of the junction model (Figure 1.5) were constructed depicting the surface temperature distribution and a typical cross-sectional area temperature distribution. These plots were constructed for the various junction areas and are shown in Figures 2.3 through 2.9 in decreasing size of powered junction area. The T_{CC} and q_C values were held at 60°C and 1.5 watts, respectively.

In order that the experimental results obtained with an IR microscope could be compared with computed data, a plot of the surface thermal resistance (θ_{SA-CC}) as a function of surface area was made for $A_J = 1.12$ mils^2 (Figure 2.10). (1.12 mils^2 was selected because it approximates the A_J of the thermal test chip.) The surface area, in this case, was correlated to a circular area by using an equivalent diameter defined from

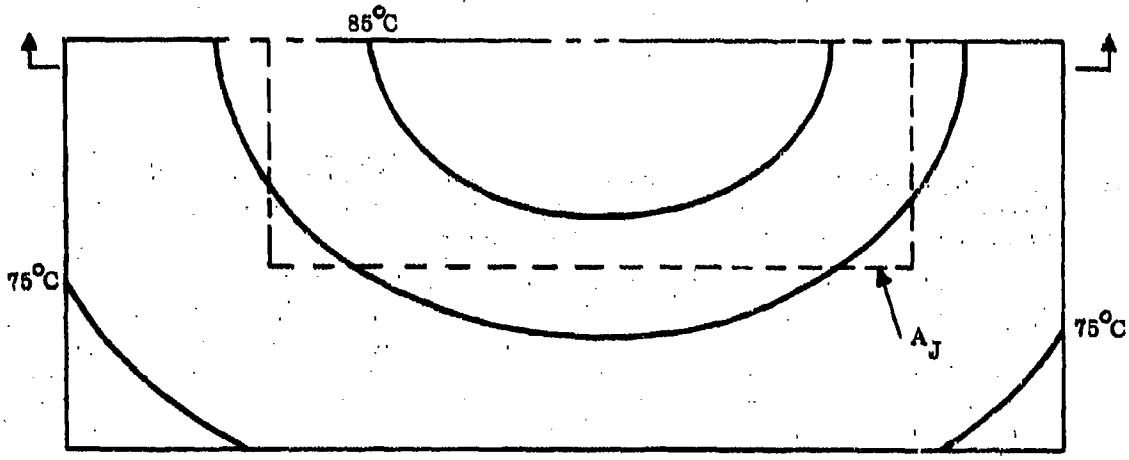
$$D_e = \sqrt{4A_S/\pi}$$

This equivalence was used because the IR microscope detects radiation from a circular area which is related to the so called "spot size" of the IR lense. Figure 2.10 shows the estimated range of readings for 15x, 36x, and 74x objective lenses. This range concept derives from the fact that the objective lense is above the surface to be measured and will receive IR radiation from the surface out to an estimated three diameters of the "spot size" of the lens; that is, it receives energy from a surface that is much larger than the specified "spot size", or half-power receiving diameter of the lense.

To obtain a useful tool for predicting the IR measurements for any junction area, within the limits of the data given, this range concept can be applied to Figure 2.11, where the plots of the data, θ_{SA-CC} and D_e, for all the various-sized junction areas have been superimposed.

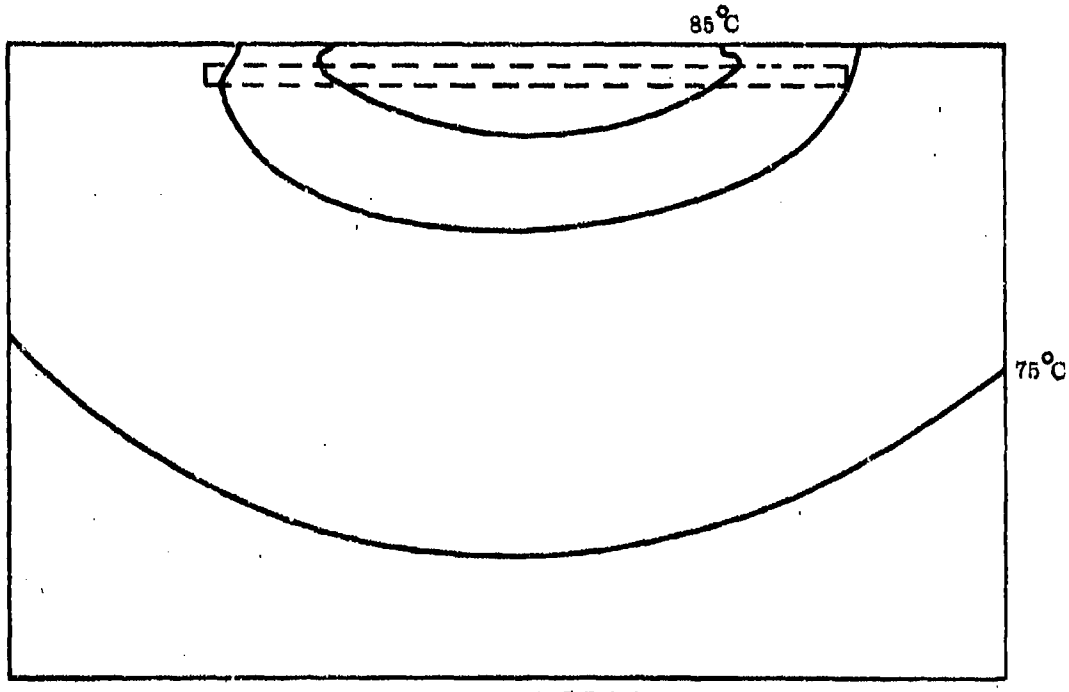
2.1.2.3 Increasing Temperature Effects

In order to see the effect on the thermal resistance values caused by raising the chip-carrier temperature, the chip-carrier temperature was simulated at 60°C, 156°C, and 257°C in the chip model and the junction region temperature was determined. This value was then used in the junction region model to determine the junction peak temperature. The various values of thermal resistance for each junction area were calculated at each chip-carrier temperature using a power dissipation of 1.5 watts. The results of the simulation are plotted in Figure 2.12, showing the rising trend of the thermal resistance values as the chip-carrier temperature is increased; it also is clear that the smaller the area the larger this increase will be. The same results are plotted in Figure 2.13 as a function of junction area, showing the decreasing value of thermal resistance for increasing junction size at various chip-carrier temperatures.



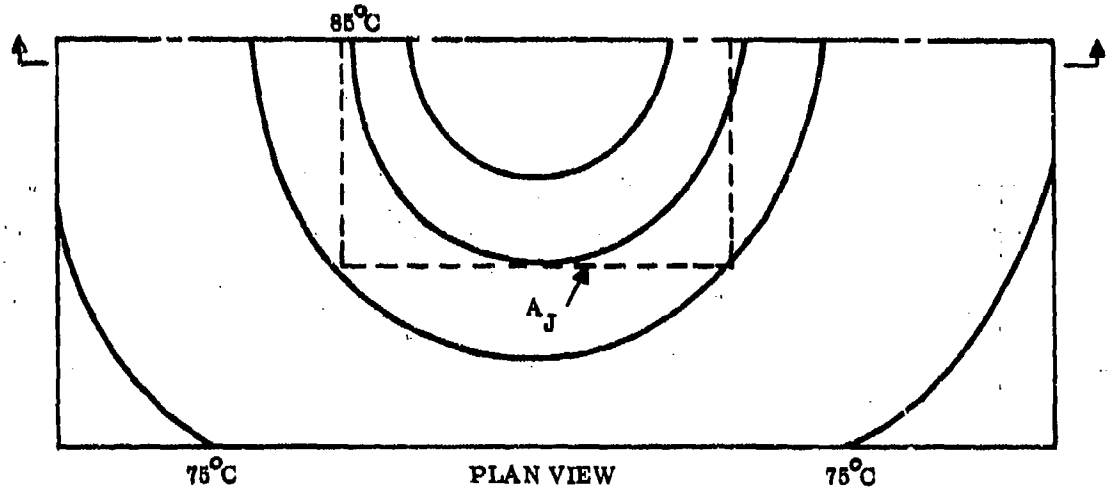
PLAN VIEW

JUNCTION MODEL



CROSS SECTION

Figure 2.3 Isothermal Plot, $A_J = 10.92$ mils^2
$T_{CC} = 60^\circ C$, $\dot{q}_C = 1.5$ Watts, Contour Interval = $5^\circ C$



JUNCTION MODEL

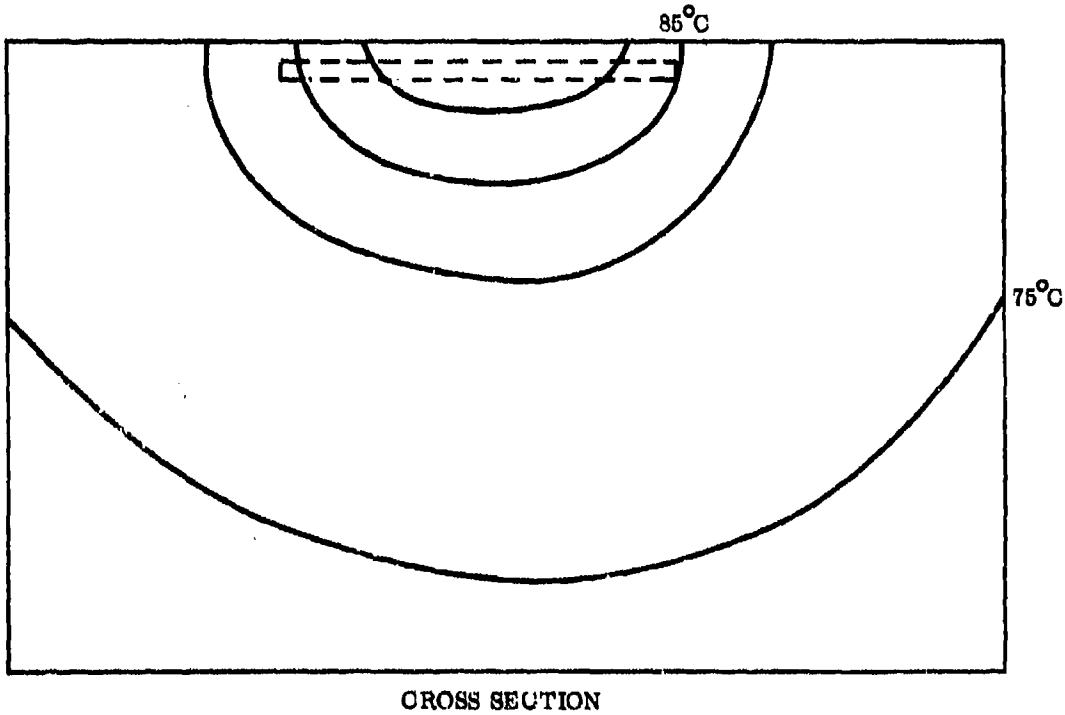
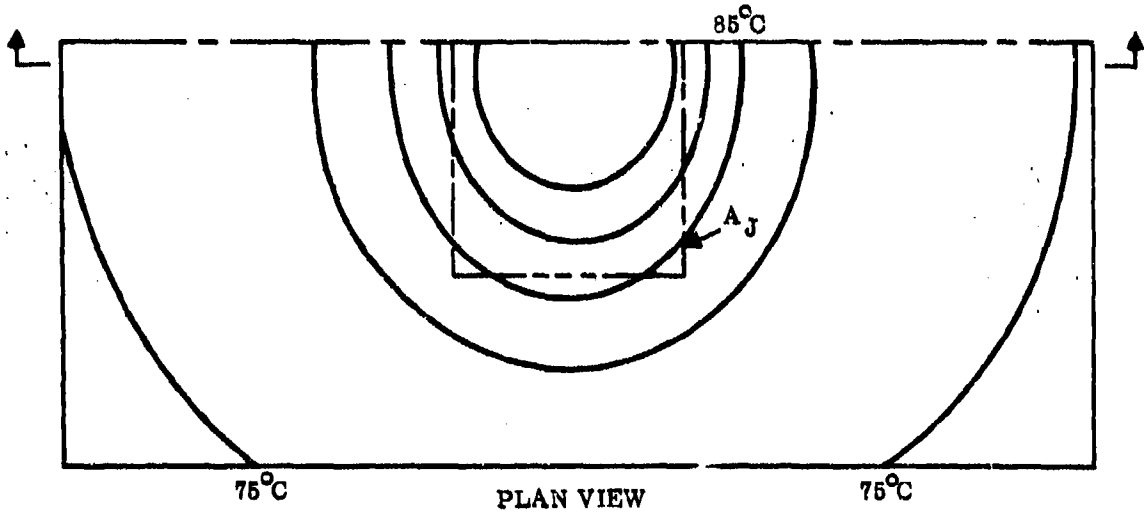
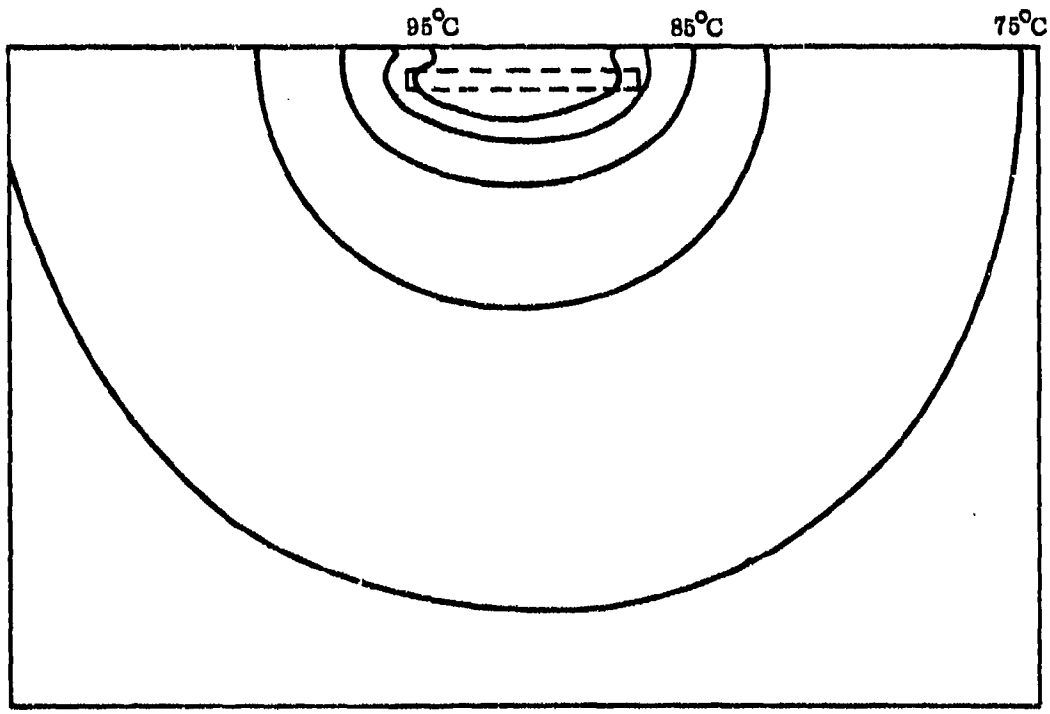


Figure 2.4 Isothermal Plot, $A_J = 6.86$ mils^2
$T_{CC} = 60^{\circ}C$, $q_C = 1.5$ Watts, Contour Interval = $5^{\circ}C$



PLAN VIEW

JUNCTION MODEL



CROSS SECTION

Figure 2.5 Isothermal Plot, $A_J = 4.05\ mil^2$
$T_{CC} = 60^{\circ}C$, $\dot{q}_C = 1.5$ Watts, Contour Interval = $5^{\circ}C$

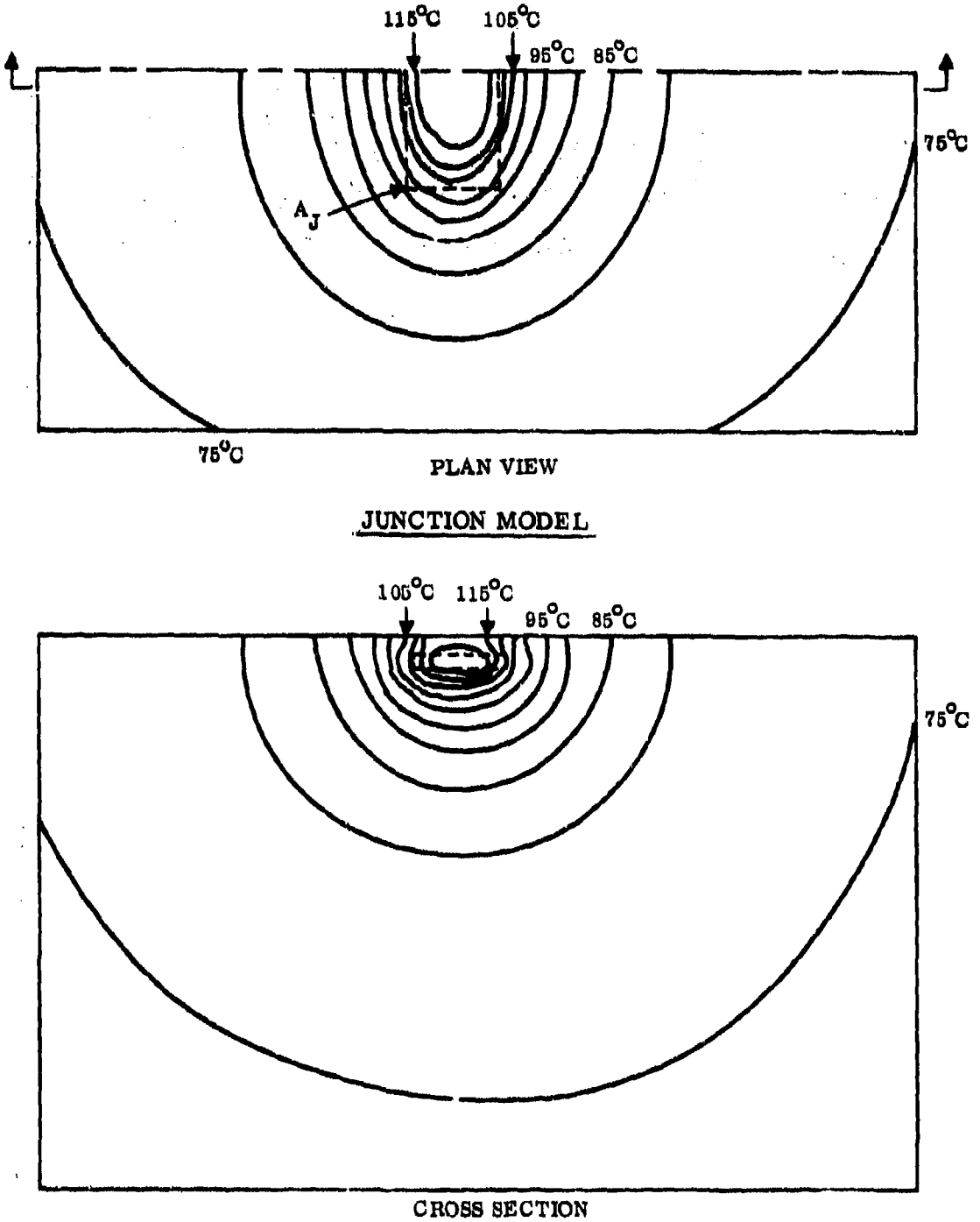
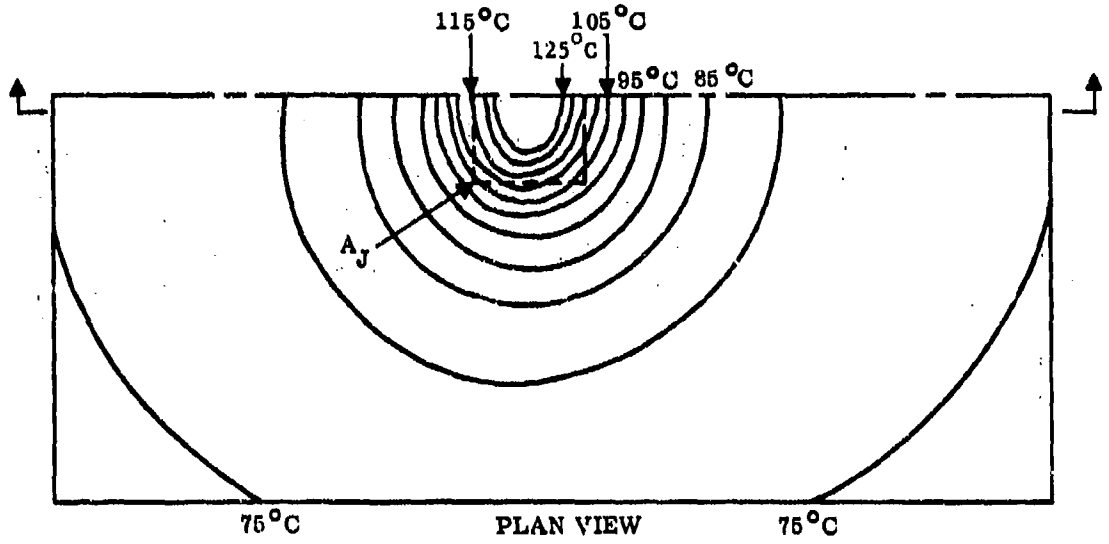


Figure 2.6 Isothermal Plot, $A_J = 1.12$ mils^2
$T_{CC} = 60^\circ C$, $q_C = 1.5$ Watts, Contour Interval = $5^\circ C$



JUNCTION MODEL

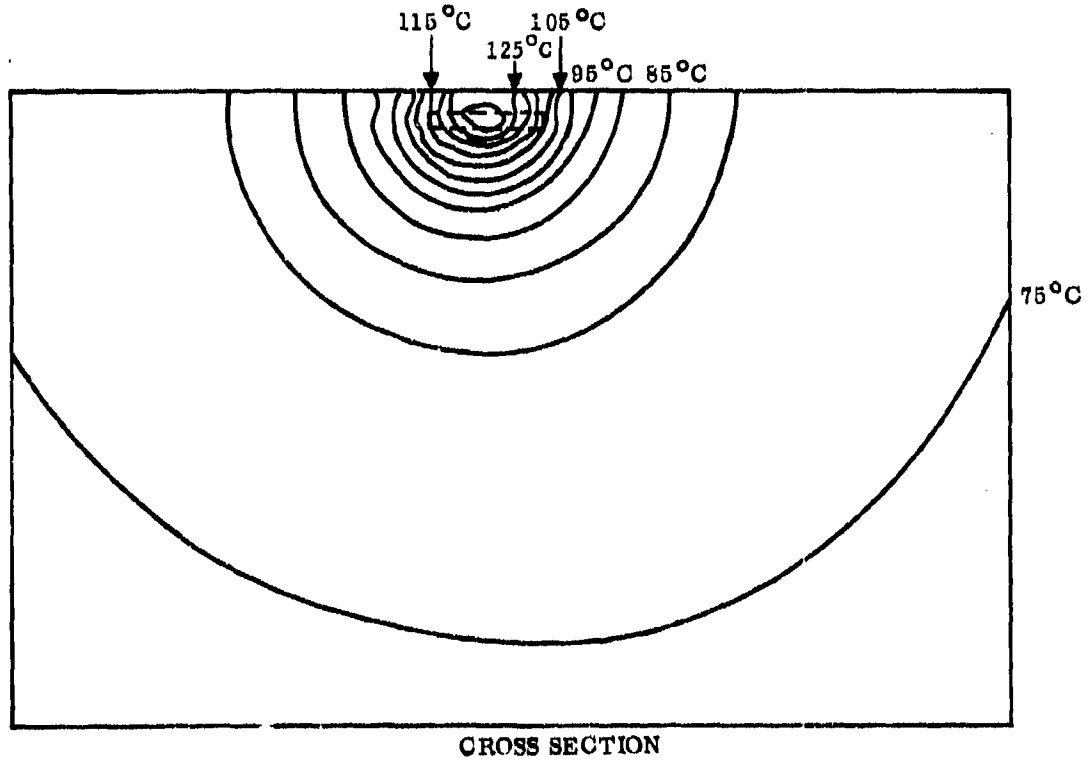
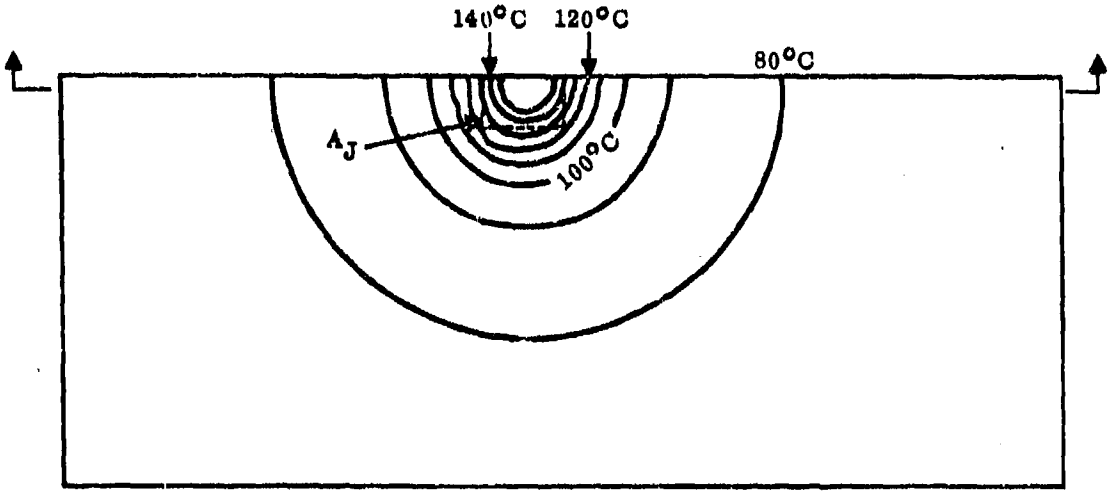
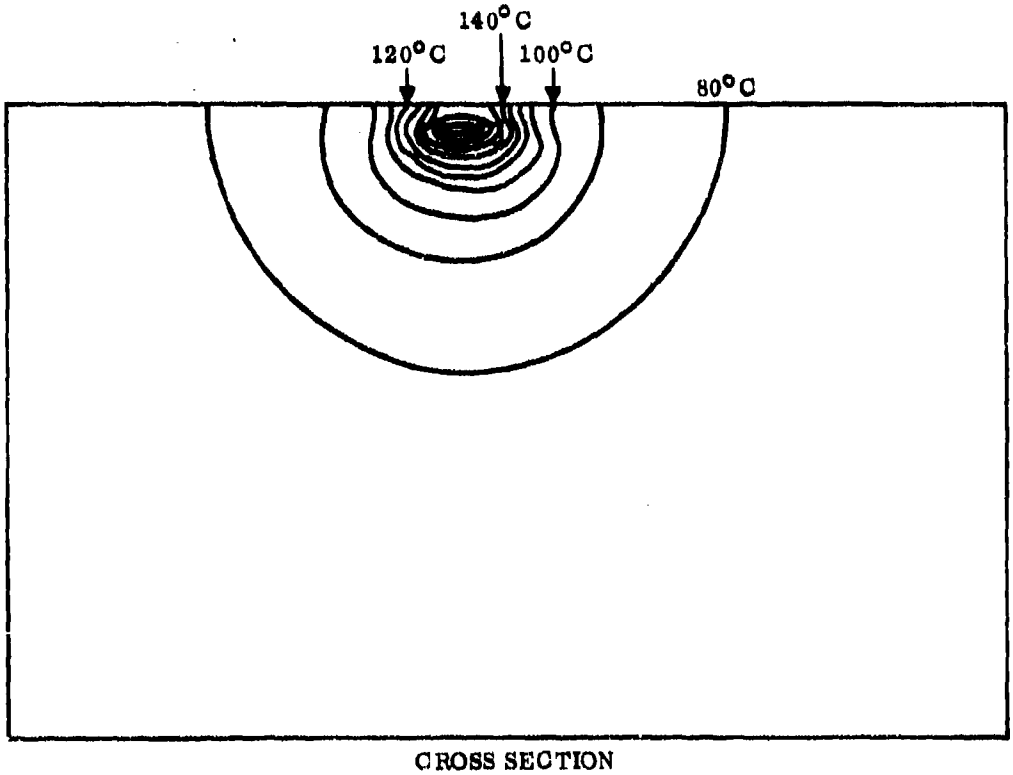


Figure 2.7 Isothermal Plot, $A_J = 0.84$ mils^2
$T_{CC} = 60^{\circ}C$, $\dot{q}_C = 1.5$ Watts, Contour Interval = $5^{\circ}C$



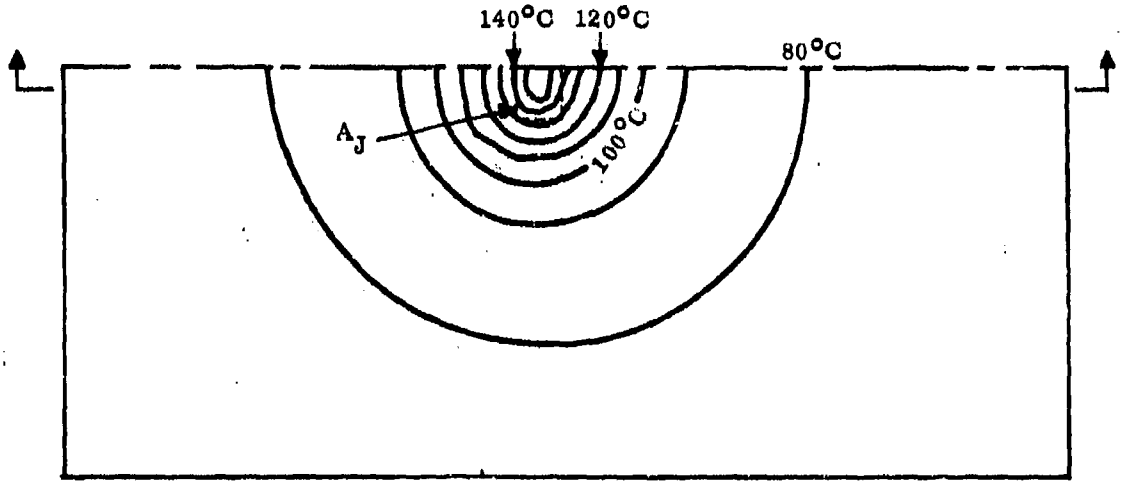
PLAN VIEW

JUNCTION MODEL



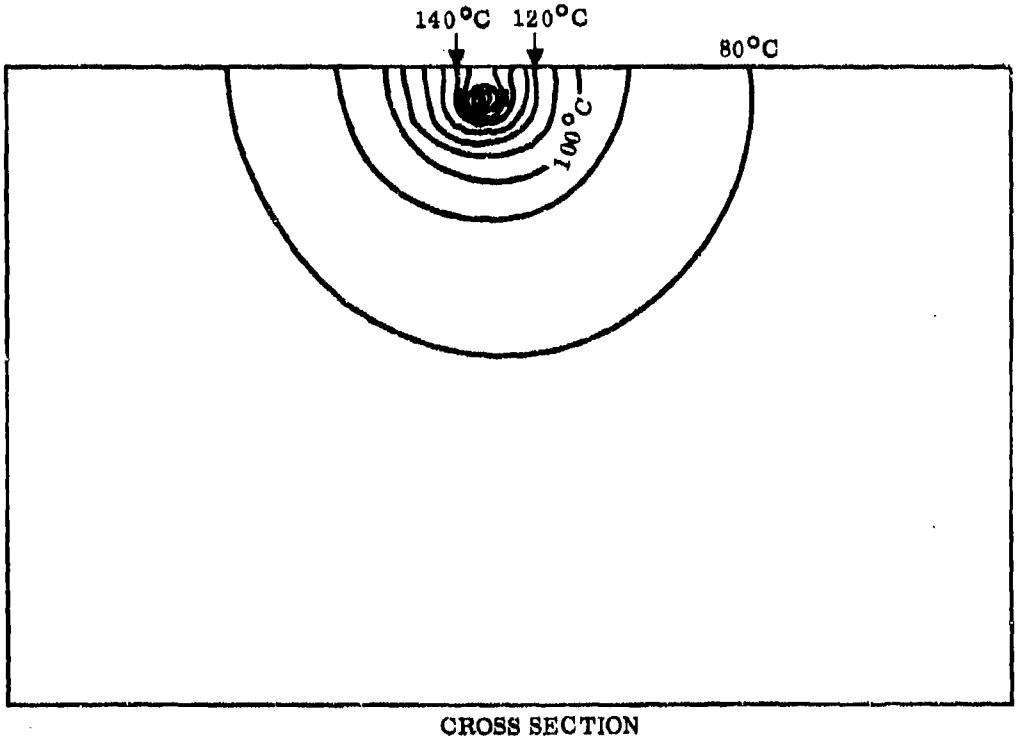
CROSS SECTION

Figure 2.8 Isothermal Plot, $A_J = 0.30$ mil^2
$T_{CC} = 60^{\circ}C$, $\dot{q}_C = 1.5$ Watts, Contour Interval = $10^{\circ}C$



PLAN VIEW

JUNCTION MODEL



CROSS SECTION

Figure 2.9 Isothermal Plot, $A_J = 0.18$ mils^2
$T_{CC} = 60^{\circ}C$, $\dot{q}_C = 1.5$ Watts, Contour Interval = $10^{\circ}C$

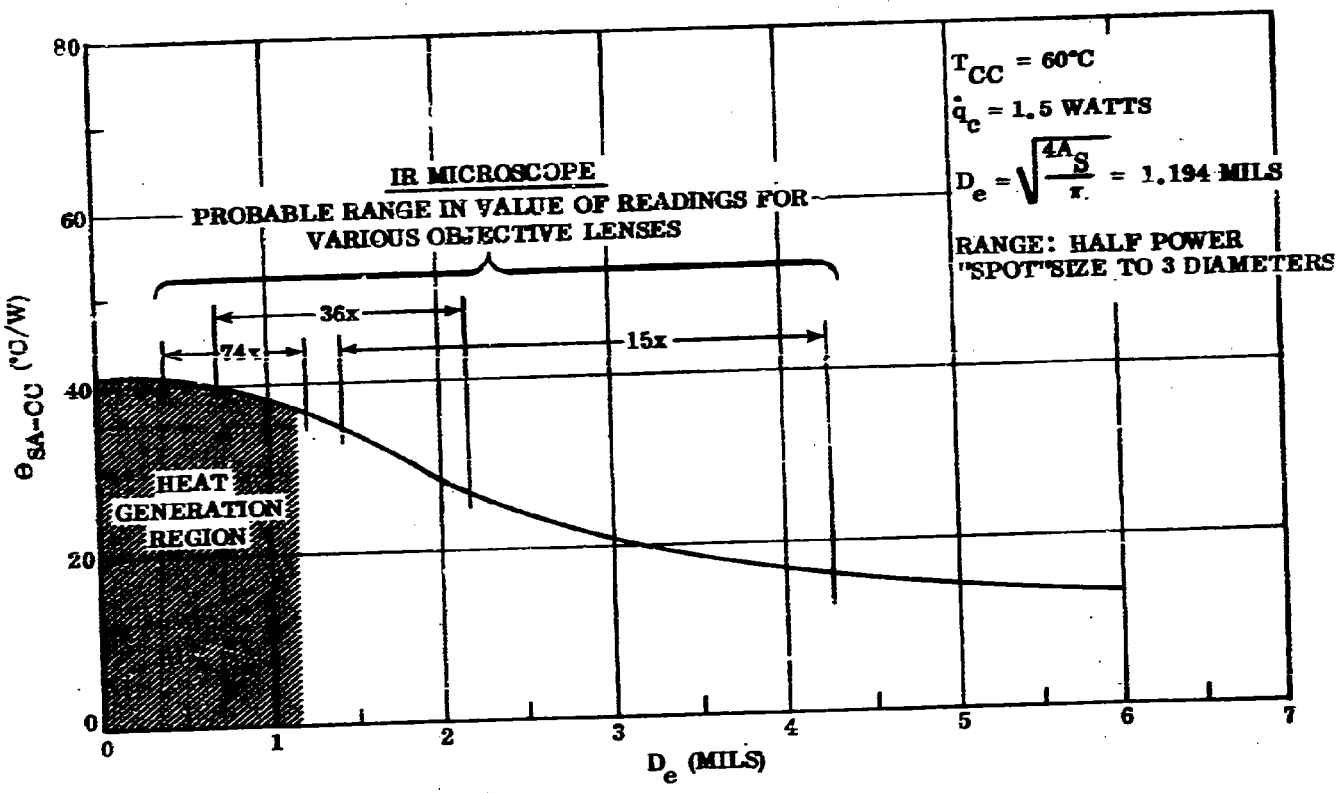


Figure 2.10 Comparison of Average Surface Thermal Resistance as a Function of Surface Area (in terms of equivalent diameter) for a Junction Size of A_J = 1.12 mils^2

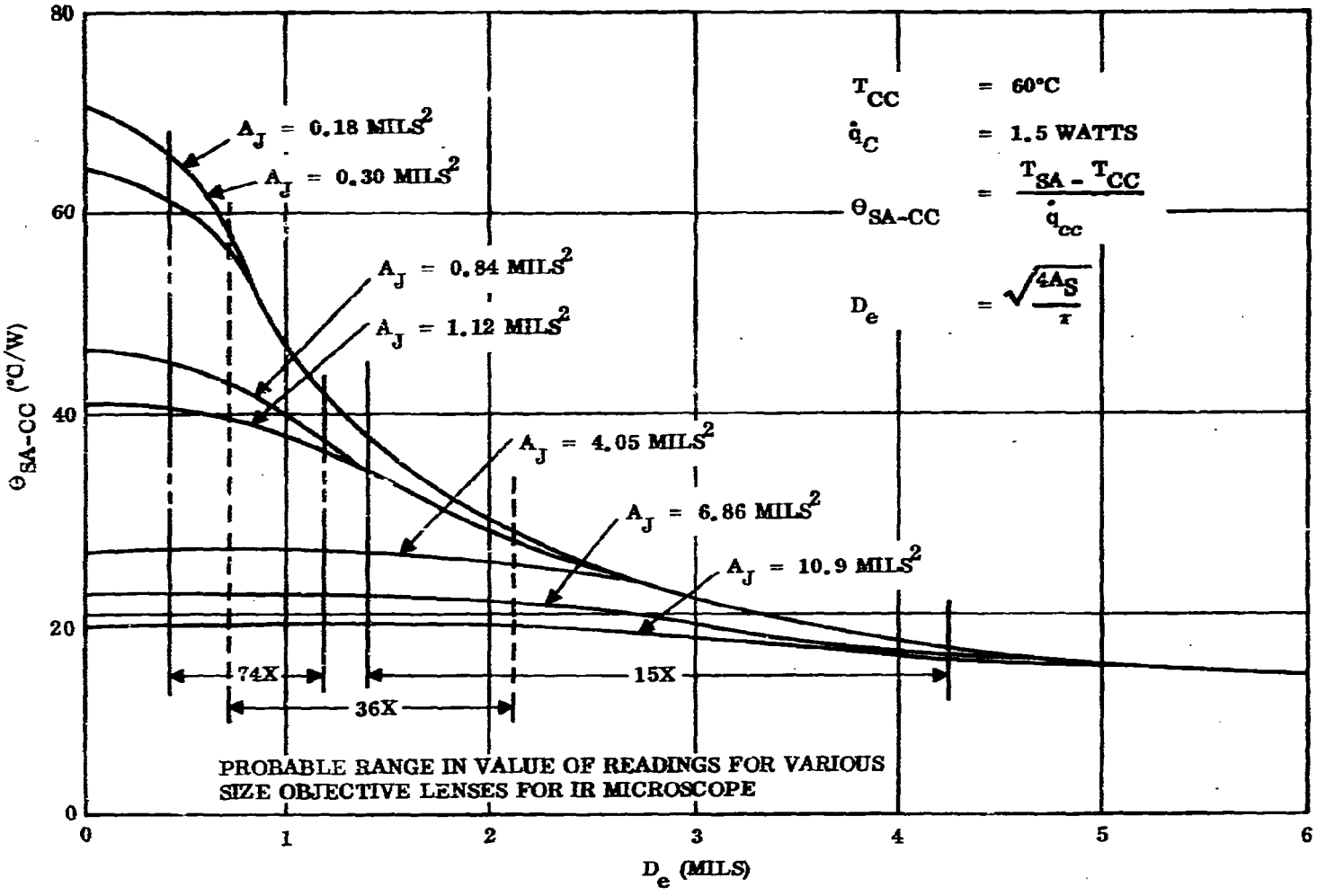


Figure 2.11 Comparison of Average Surface Thermal Resistance as a Function of Surface Area (in terms of equivalent diameter) for Different Size Junction Areas

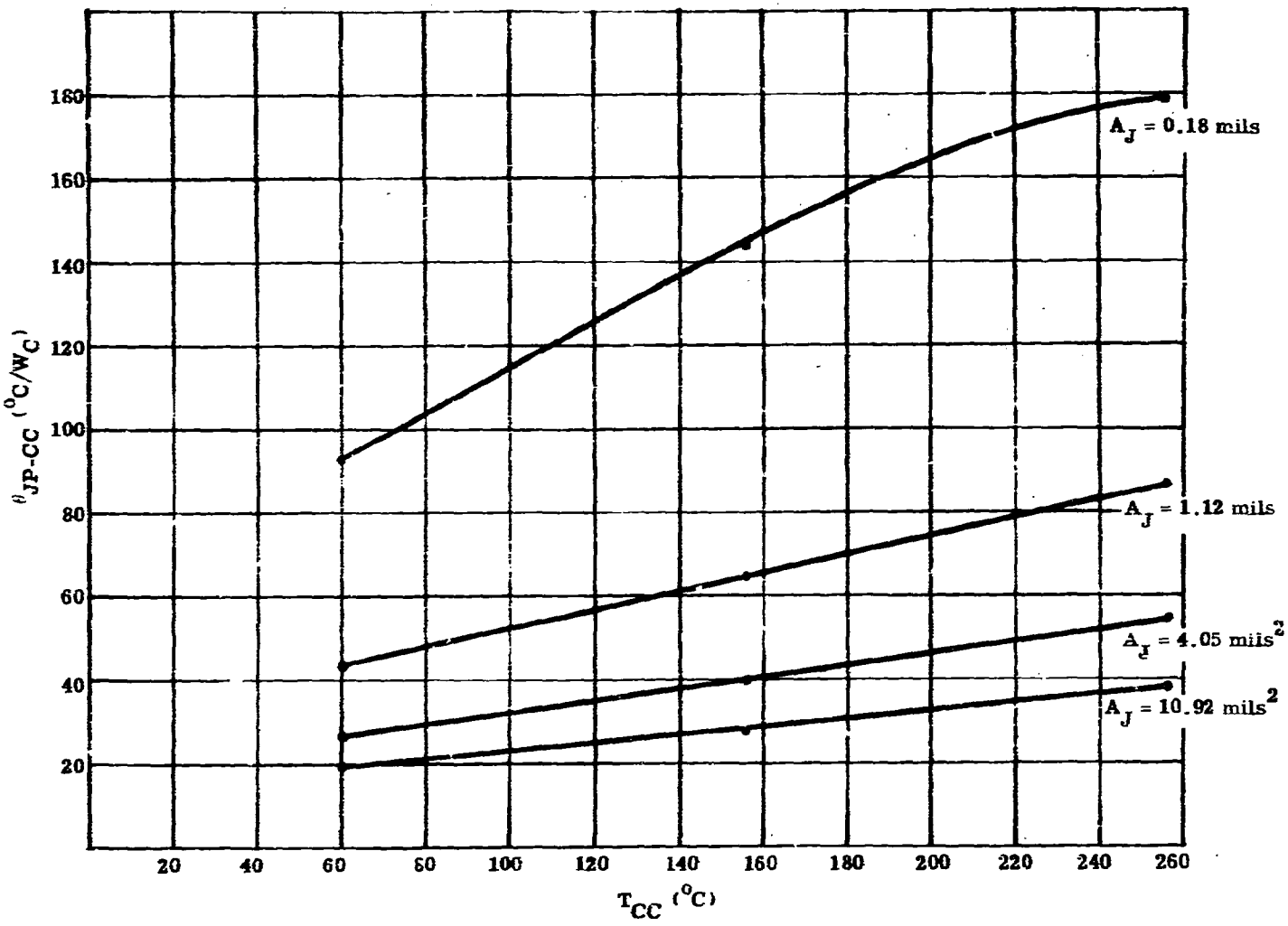


Figure 2.12 Comparison of Thermal Resistance vs Chip Carrier Temperature for Various Junction Areas

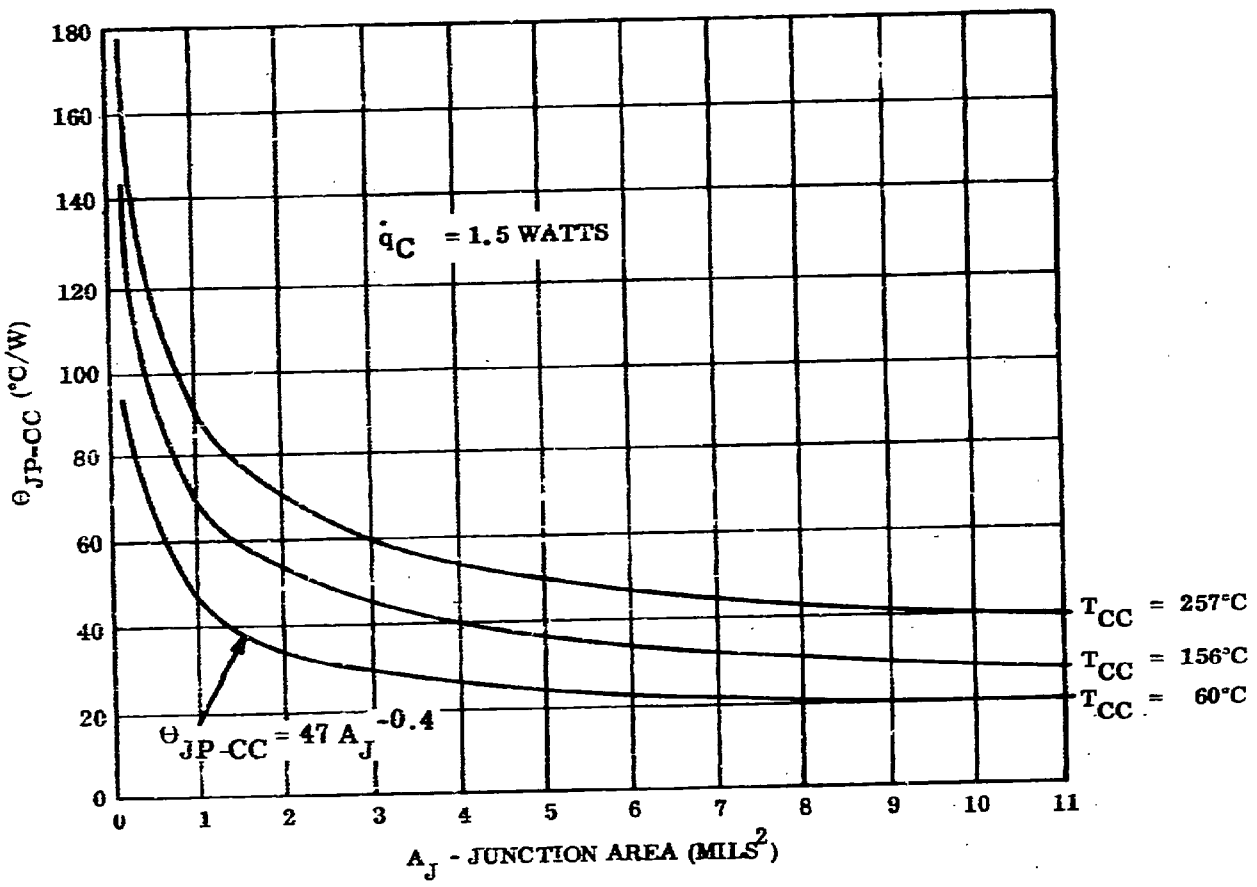


Figure 2.13 Comparison of Thermal Resistance as a Function of Junction Area at Various Chip Carrier Temperatures

2.1.2.4 Variation of Thermal Resistance Values with Power Dissipation Rate

In order to observe the effects of varying the power dissipation, the power was input at 0.5, 1.5, and 2.5 watts for selected junction area sizes. For these cases the chip carrier temperature was held at 60°C. Figure 2.14 shows the results of this simulation, indicating a rising trend in thermal resistance values, and showing that the change increases with decreasing area.

2.1.2.5 Thermal Time Constants Relative to Junction Size

The transient temperature response of selected junction areas was computed and is shown in Figure 2.15. From these curves the relative thermal time constants can be determined. The relative thermal time constant τ_{JP-JR} is defined as the time required for the junction peak temperature rise, relative to the junction region temperature, to reach 63.2% of its final steady state value after a step function in power dissipation is applied. The thermal time constants, determined from Figure 2.15, are plotted in Figure 2.16 against junction size to show the relative effect of junction size on the thermal time constant.

2.1.3 Theoretical Conclusions

The thermal resistance values θ_{JP-CC} and θ_{JA-CC} decrease exponentially as the junction size increases (Table 2.1 and Figure 2.2).

The surface temperature variation and, thus, the possible range in thermal resistance values which could be measured with an IR microscope, increases significantly as the junction size decreases (Figures 2.10 and 2.11). For example in Figure 2.11 for a powered junction size of $A_J = 0.18$ mil^2, a surface temperature measured with a 74x objective lens might yield a thermal resistance value from about 70°C/W from a 0.7 mil (half power spot size surface area) to 42°C/W from a 2.1 mil diameter area (three times the half-power spot size). For the largest powered junction area considered, A_J = 10.9 mils^2, the same 74x microscope would probably yield a nearly constant reading of 19°C/W since the surface temperature is fairly uniform for this large junction. These variations do not include other IR measurement effects caused by surface preparation, emissivity etc. Appendix C contains excerpts from Reference(1) in which these possible errors are discussed.

The thermal resistance, junction peak-to-chip carrier, will vary approximately with the inverse of the junction area to the 0.4 power; i.e. $\theta_{JP-CC} = 47 A_J^{-0.4}$, [°C/W$_C$] for a chip carrier temperature of 60°C.

As power is increased θ_{JP-CC} increases; the smaller the junction area the greater the increase will be (Figure 2.14). For example, with a 5/1 increase in power input, θ_{JP-CC} will increase about 4°C/W for $A_J = 10.9$ mils^2, while, for $A_J = 0.18$ mils^2, the increase in θ_{JP-CC} is about 41°C/W.

The relative thermal time constant, τ_{TP-JR}, will vary approximately with the junction area to the 0.45 power, i.e. $\tau_{TP-JR} \approx 3.44 A_J^{0.45}$ μsec over the range of junction areas used.

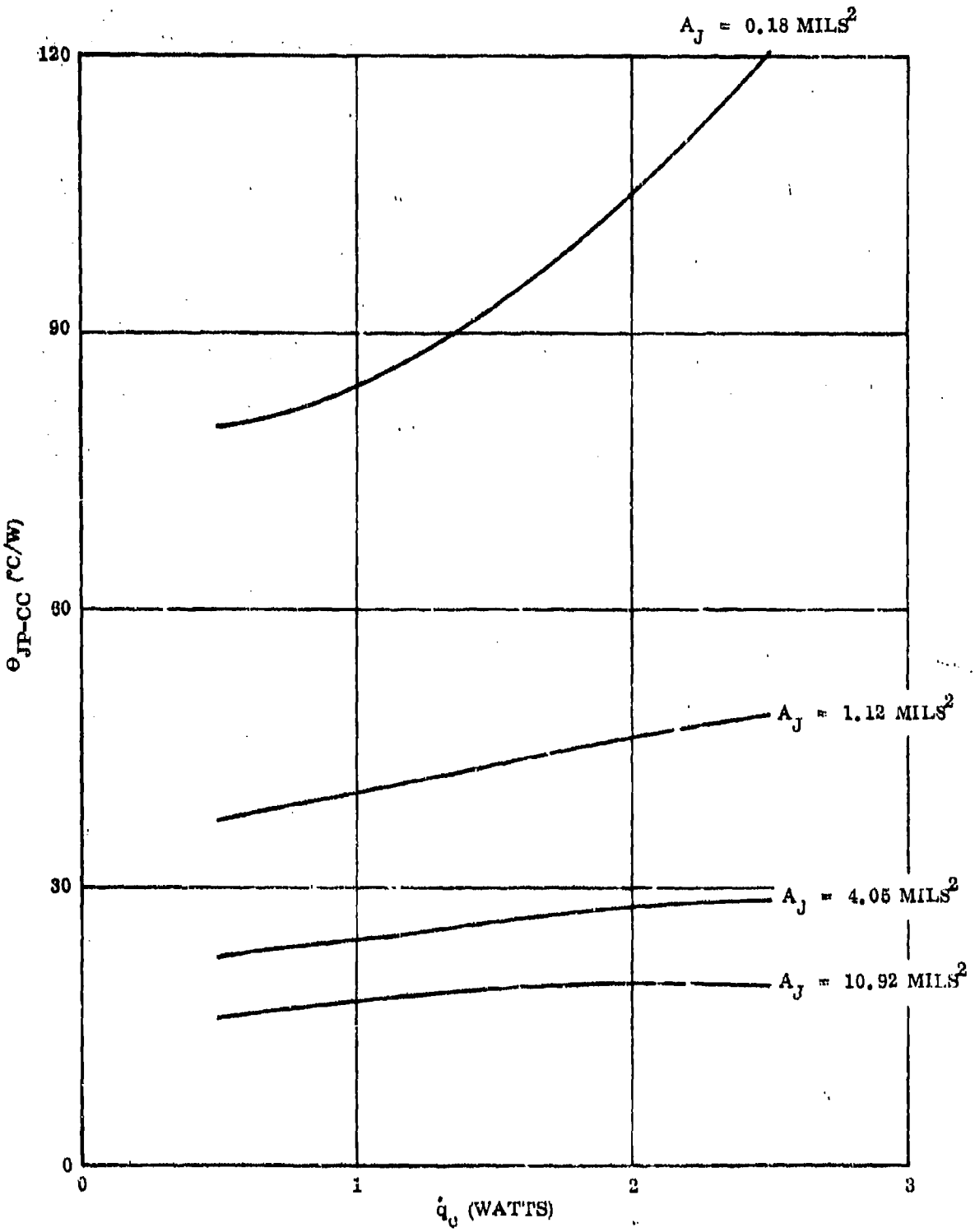


Figure 2.14 Comparison of Thermal Resistance (θ_{JP-CC}) as a Function of Input Power for Various Junction Areas

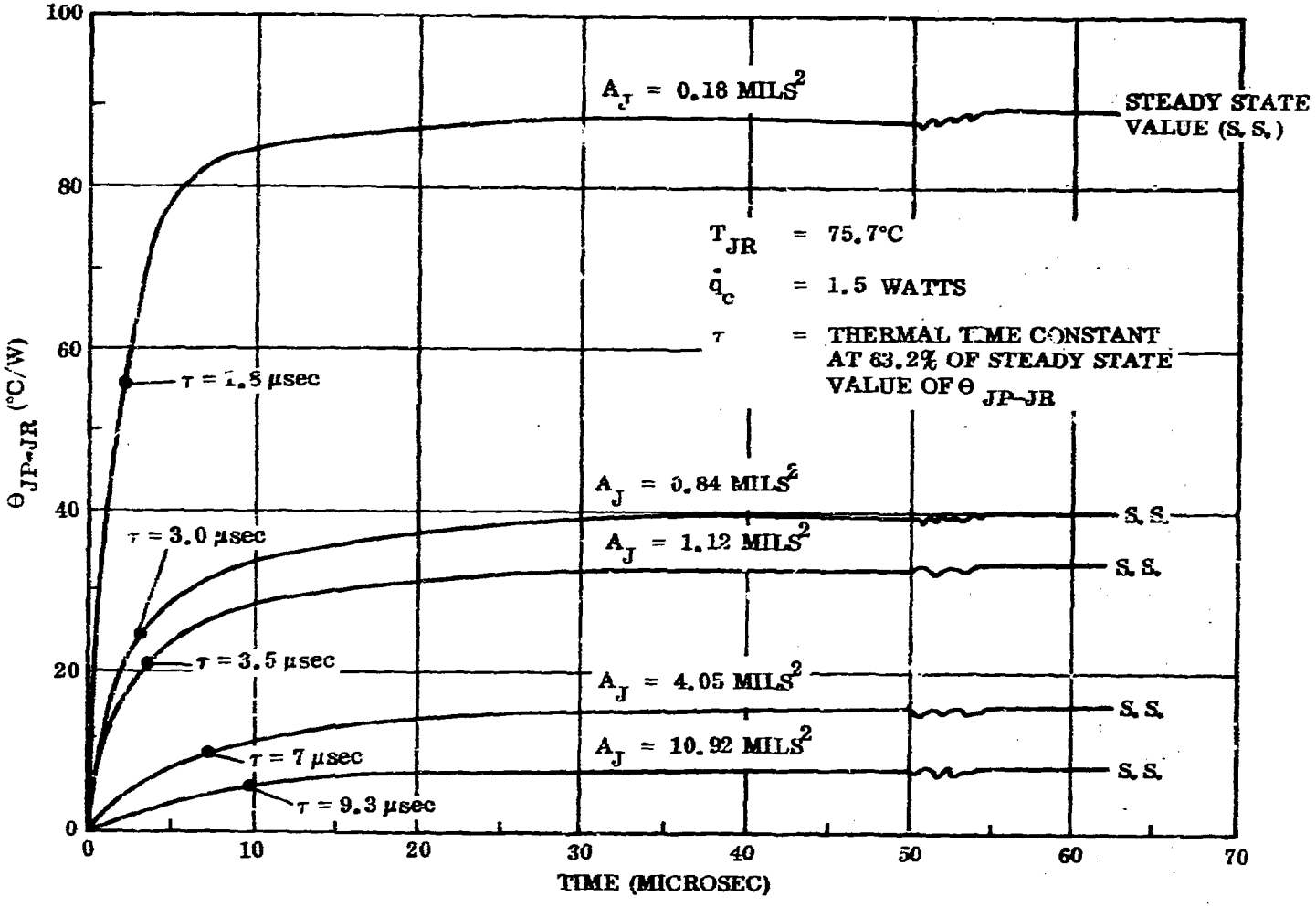


Figure 2.15 Transient Temperature Response Relative to Junction Region Temperature for Various Junction Areas

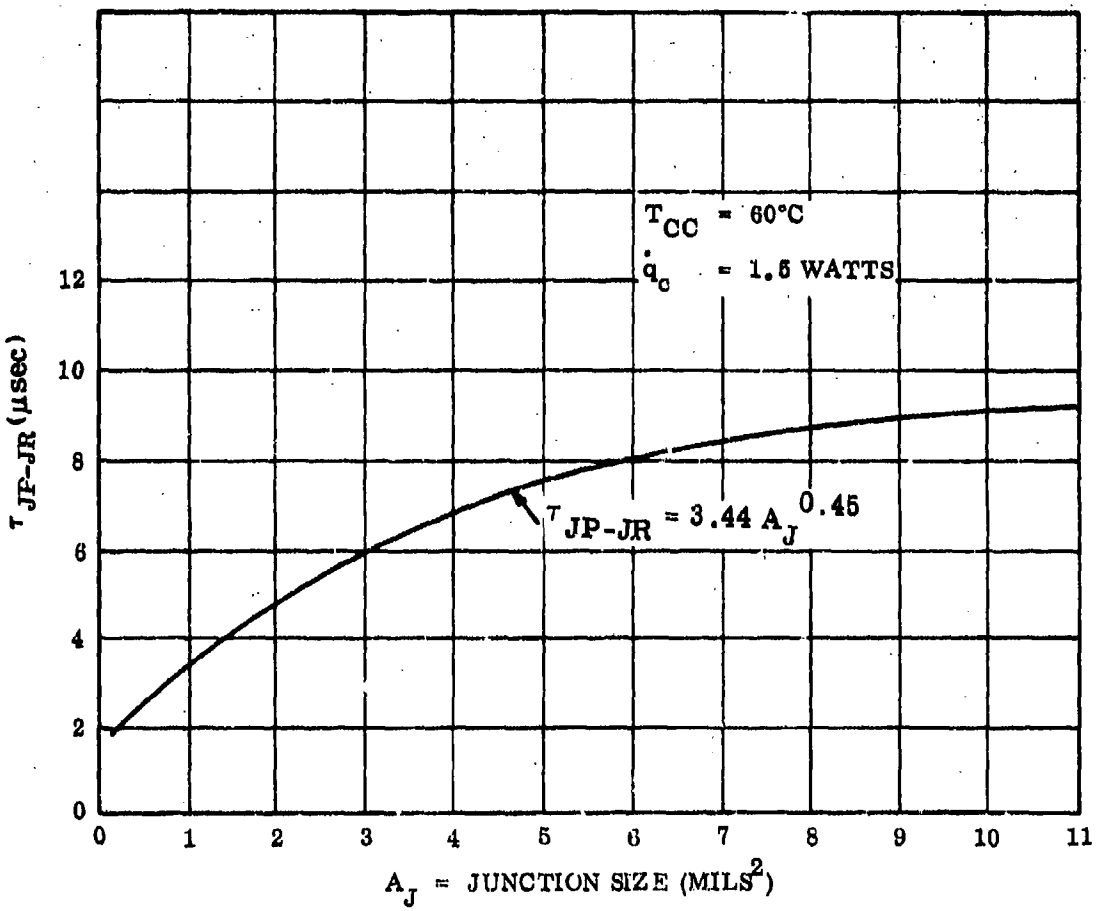


Figure 2.16 Comparison of Thermal Time Constant (τ_{JP-JR}) as a Function of Junction Size

$T_{CC} = 60^{\circ}C$

$\dot{q}_C = 1.5$ Watts

2.2 EXPERIMENTAL MEASUREMENTS

2.2.1 Objectives

The objective of the experimental measurements was to determine methods for improving the IR measurements of the surface temperatures of microcircuits and to improve the method of making electrical measurements of the junction temperature.

To accomplish this objective, tests were conducted with a high resolution objective lens on the IR microscope, a study for improving coating techniques was made, and a test fixture was built to improve electrical measurements of junction temperature. In addition, thermal time constants, pulsed power effects, and variations in peak temperature, with a still-air and forced-air ambient, were made on representative devices, together with the thermal characterization of I^2L devices.

2.2.2 Improved Coating Techniques

A study of improved coating techniques for infrared measurements was done in conjunction with work being performed under a National Science Foundation Grant. A technique that led to coatings with emissivities as high as 98% was developed. These coatings, while not completely transparent, permit one to observe the metallization pattern underneath; this is a great aid in locating the hot spot (or spots) to be measured. Appendix D is a copy of the Final report on the work; it describes the coatings in detail.

The optimum coating consists of fine glass particles suspended in Sodium Silicate. When dry it is semi-opaque but wetting the coating with a volatile liquid renders it nearly completely transparent to visible light by suppressing scattering and surface reflections. This coating was used in the infrared measurements described herein.

Figure 2.17 shows the spinner device used to apply the coatings. Figure 2.18 shows the thermal test chip with a coating, and Figure 2.19 shows the same chip after a drop of alcohol has been applied to the coating.

2.2.3 High Resolution Infrared Measurements

Tests were conducted with the SCP 14 test chips mounted in F-1 packages, which had been used in the earlier program [1]. The test set-up is shown in Figure 2.20.

A 74x objective with half-power resolution of 0.4 mils, for the Barnes Infrared Radiometer was purchased from the vendor: The stated working distance for this objective is 0.090"; however, on receipt, it was found that this distance refers to the flat portion of the main body of the objective. A small raised portion at the housing surrounding the antenna pupil protrudes some 0.040", which, in effect, reduced the working distance to 0.050" because the raised land was too large to permit observation of any device other than those mounted in F style packages. These experiments were, therefore, confined to that type of package.

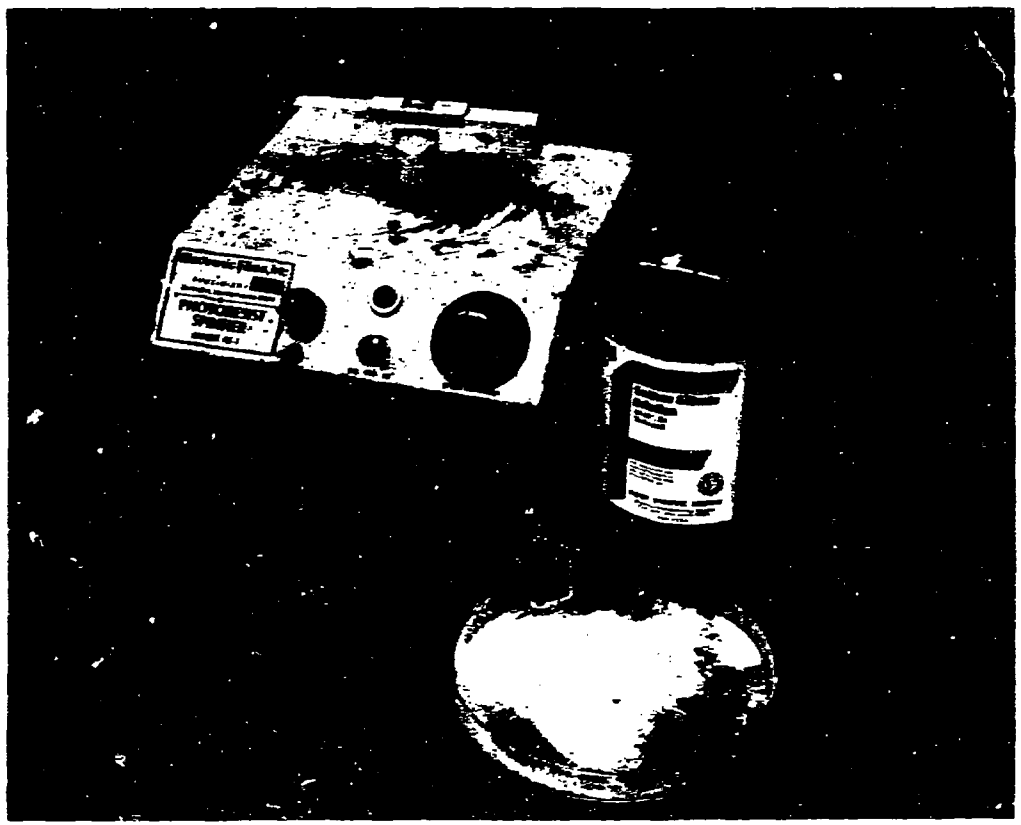


Figure 2.17 Spinner Used for Applying Coatings

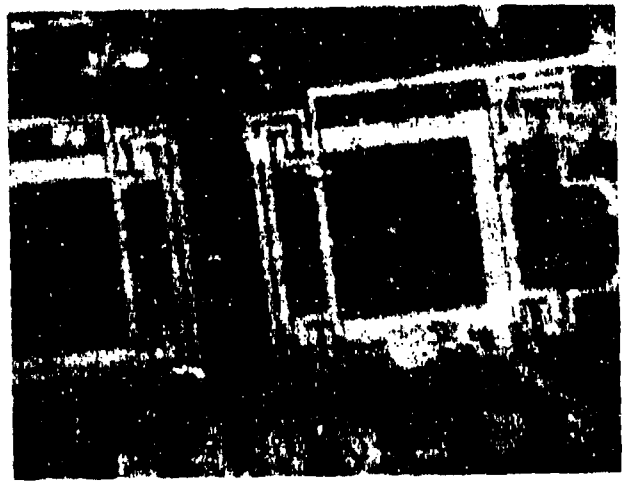


Figure 2.18 Device with Coating

Figure 2.19 Device with Coating After Application of Alcohol

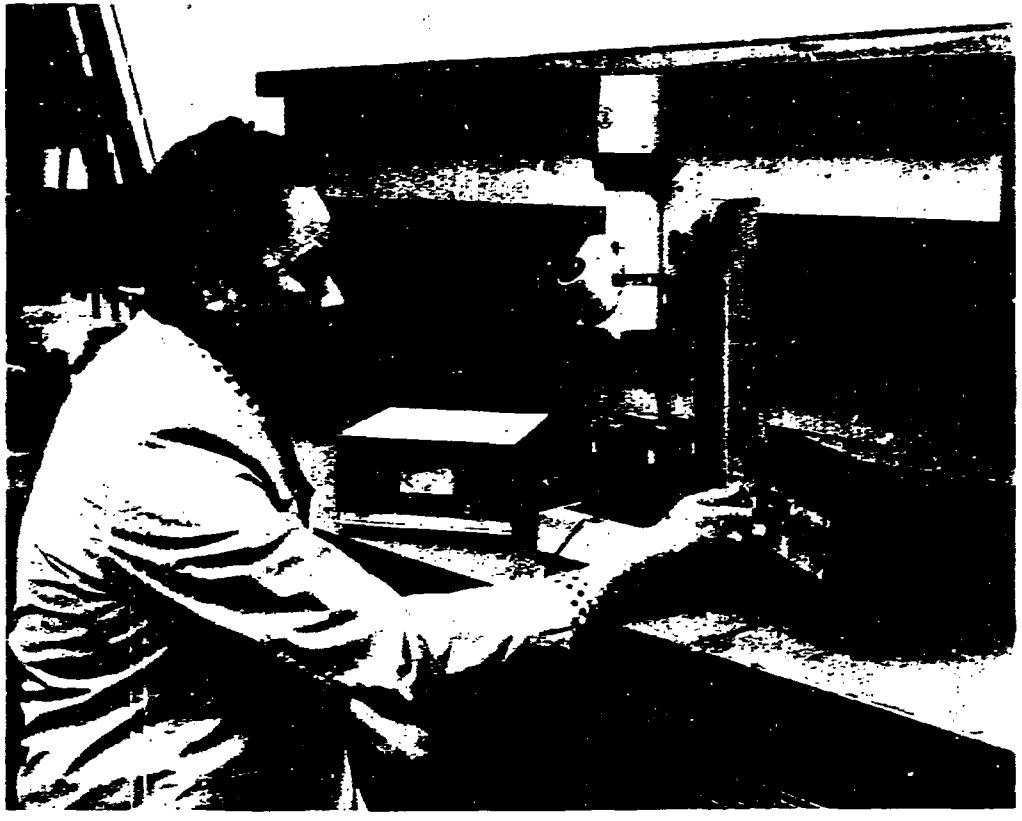


Figure 2.20 High Resolution Test Set Up

In addition, it was necessary to modify the instrument by incorporating a shutter into the body to interrupt the radiation beam in order to calibrate the instrument or permit setting it to zero. Figures 2.21 and 2.22 show the modification made to the microscope.

In normal use, an external shutter is inserted outside the objective, the instrument is set to zero, and the deflection is recorded when the shutter is removed to allow the measured radiation to enter. With such a small working distance, this would be impractical with this objective.

The shutter is made of blackened copper and has a copper-constantan thermocouple attached to allow accurate measurement of the shutter temperature. This also allows compensation for differences in internal temperature of the housing and external shutter. In practice, the emissivity of the coating did not require any correction.

The electrically powered heat sink (Figure 2.23) was used to make these measurements, allowing reasonably quick changes in heat sink temperature. The test chip was powered by applying power to the four innermost transistors. This power value was determined by measuring collector and base voltages and currents. Oscillations were avoided by placing ferrite beads on each base lead and bypassing each collector.

Readings of surface average temperatures were obtained as the power input was varied. The chip carrier temperature was measured with the thermocouple probe, which can be raised from beneath the heat sink (see Figure 2.23). A typical data plot obtained in this manner is shown in Figure 2.24. The abscissa is applied power, the ordinate is surface average temperature above that of the thermal probe. It can be seen that the points lie in a straight line, but do not pass through the origin. Linear regression was used to fit the best line to these points, and the slope is taken as the thermal resistance, which, in this figure, is 16.6°C/W. Time did not permit any detailed investigation into the zero offset. The offset indicates that the probe is actually lower in temperature than the chip carrier. One possible explanation is that heat transfer from the lower portions of the probe assembly may have caused a temperature drop across this interface. However, data taken at higher heat sink temperatures did not show large offsets. Data on the same chip at a heat sink temperature of 100°C are shown in Figure 2.25. Data were also obtained at 150°C. The actual surface average temperature at these higher temperatures was quite high. Data for these three cases are shown in Figure 2.26. The ordinate is thermal resistance (surface average-to-chip carrier) and the abscissa is the maximum chip carrier temperature as measured by the thermal probe. The rising trend can be clearly seen.

2.2.4 Transient Thermal Impedance Measurements

At the beginning of this project, we built a fixture to measure transient thermal impedance in power transistors, using the technique originated at the National Bureau of Standards. The fixture is arranged so that, at suitable intervals, it can gate off the power flow to a transistor, while continuing to supply a small measurement current to the base-emitter junction.

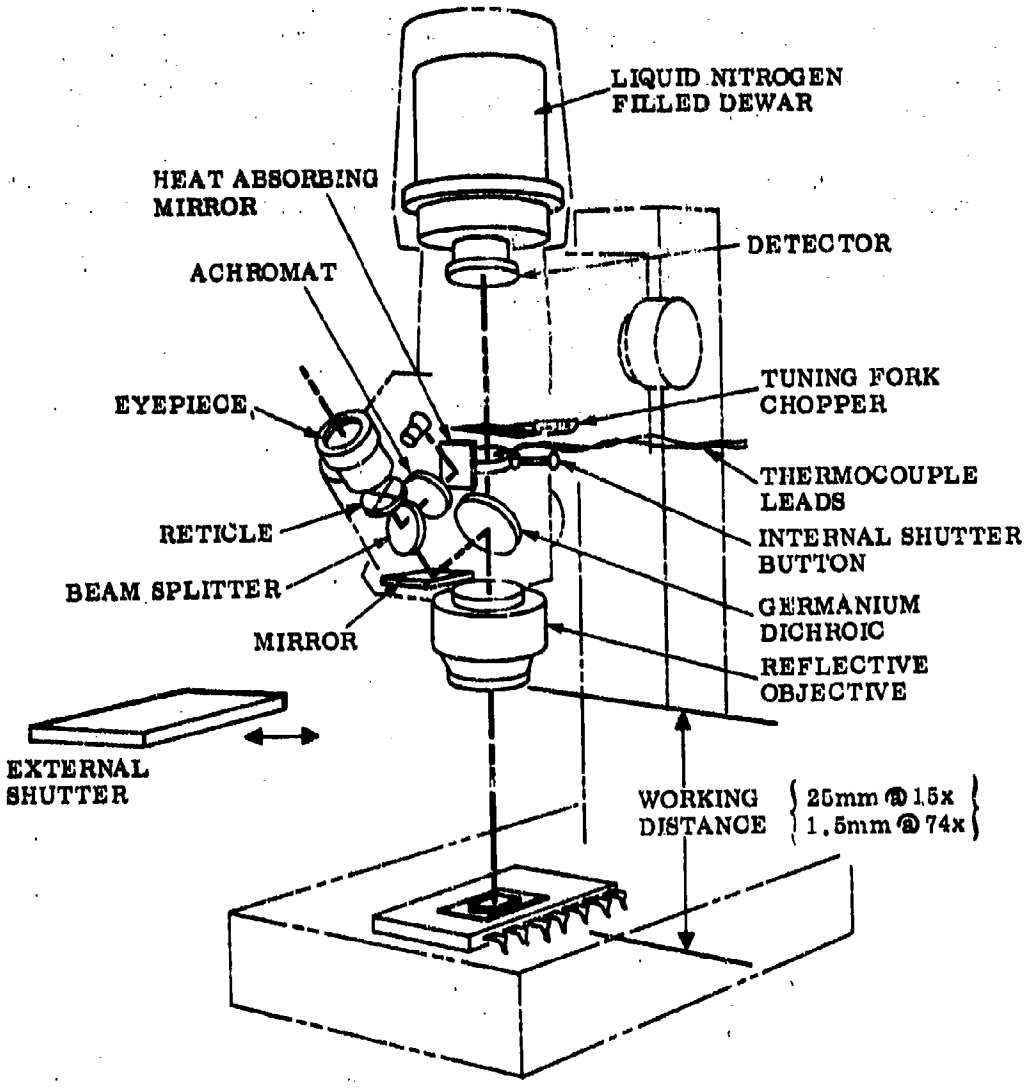


Figure 2.21 Modification to Microscope for High Temperature and High Resolution Tests

Figure 2.22 Modification of Scope

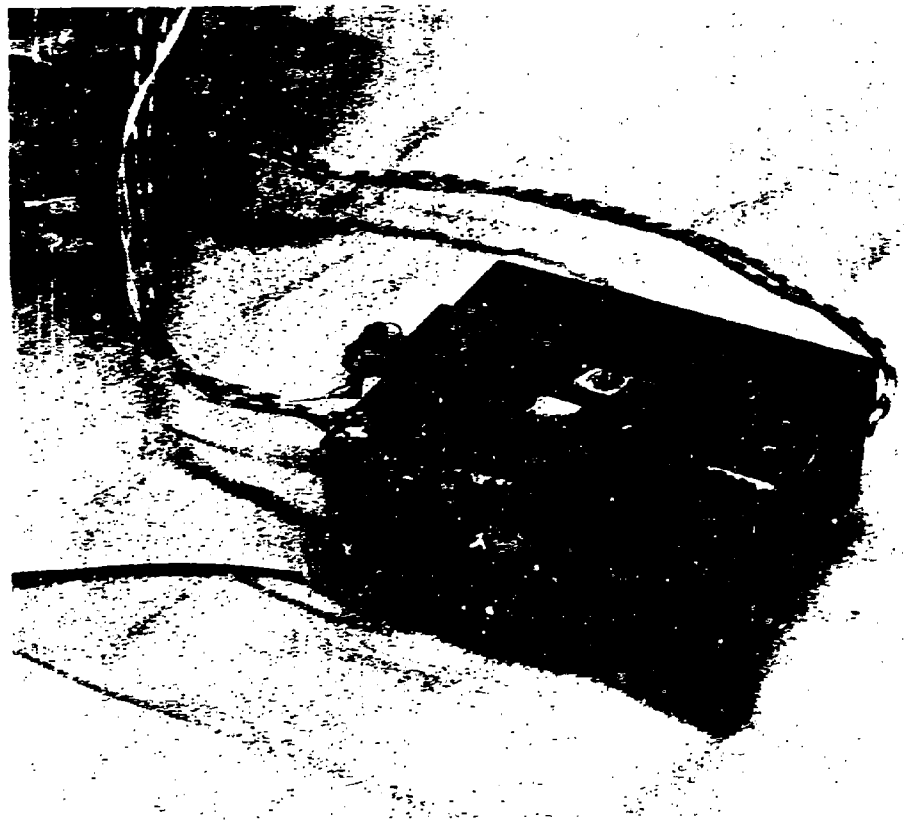


Figure 2.23 Heat Sink Assembly

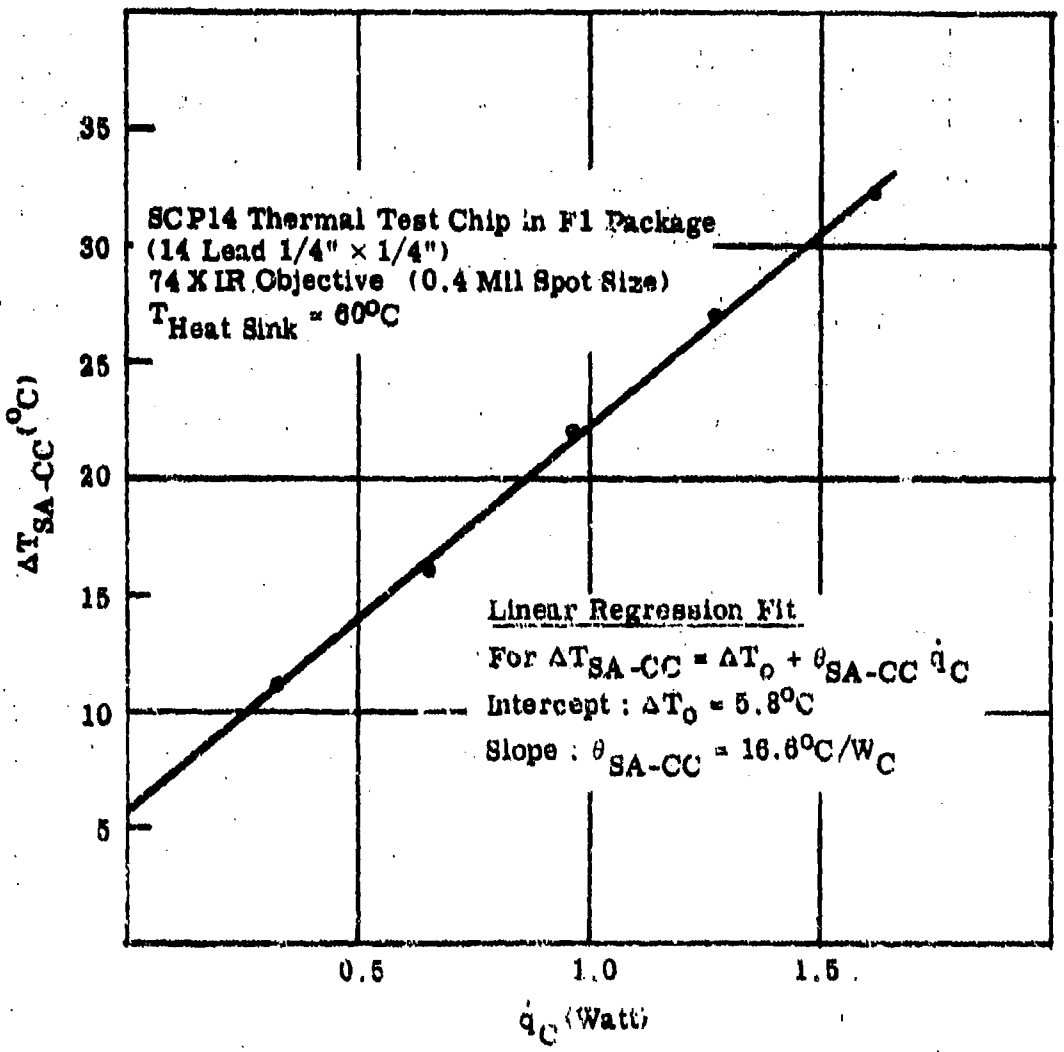


Figure 3.24 Comparison of Thermal Temperature Rise as a Function of Power Input at T_{HS} = 60°C

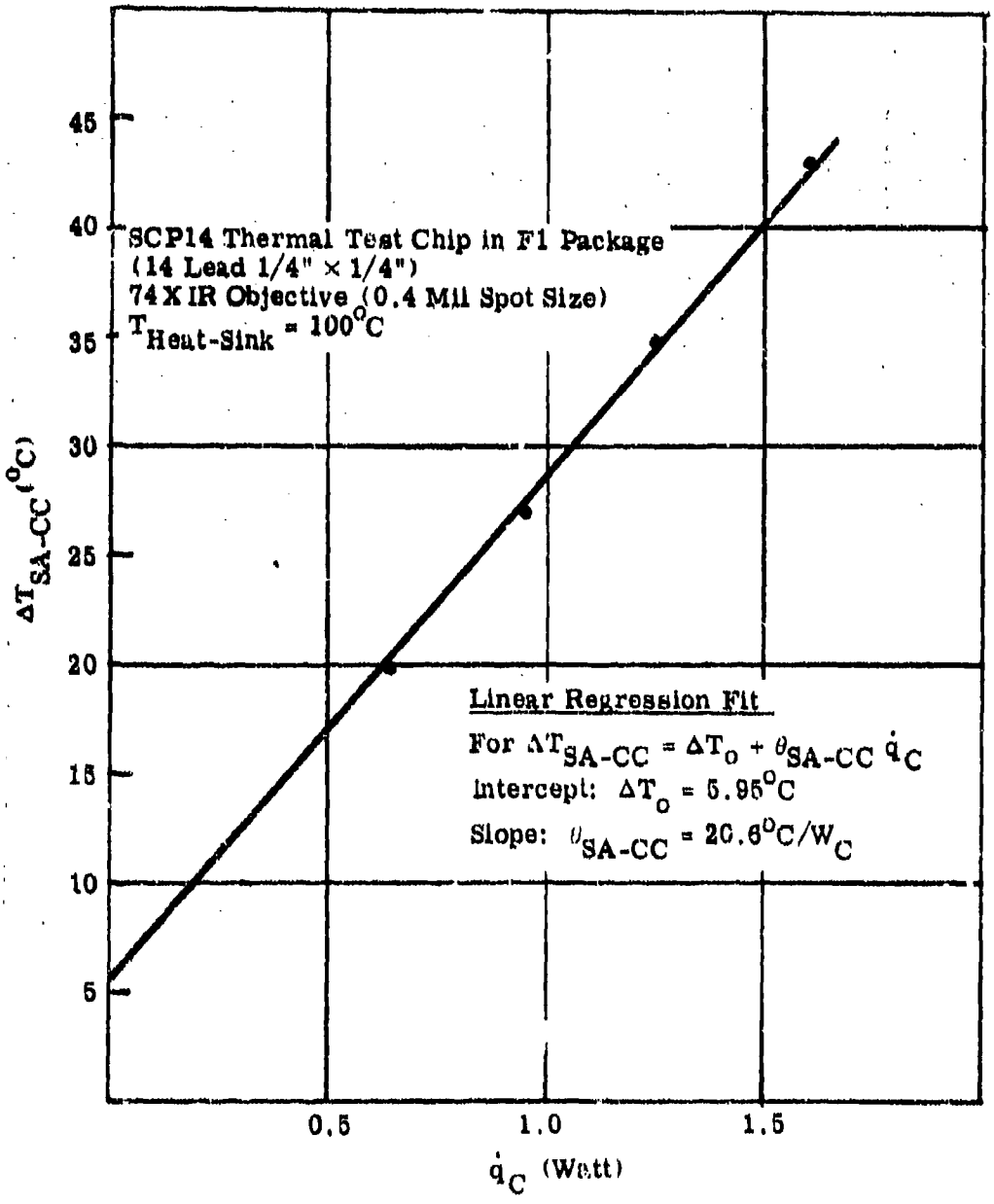


Figure 2.25 Comparison of Temperature Rise as a Function of Power Input at $T_{HS} = 100^{o}C$

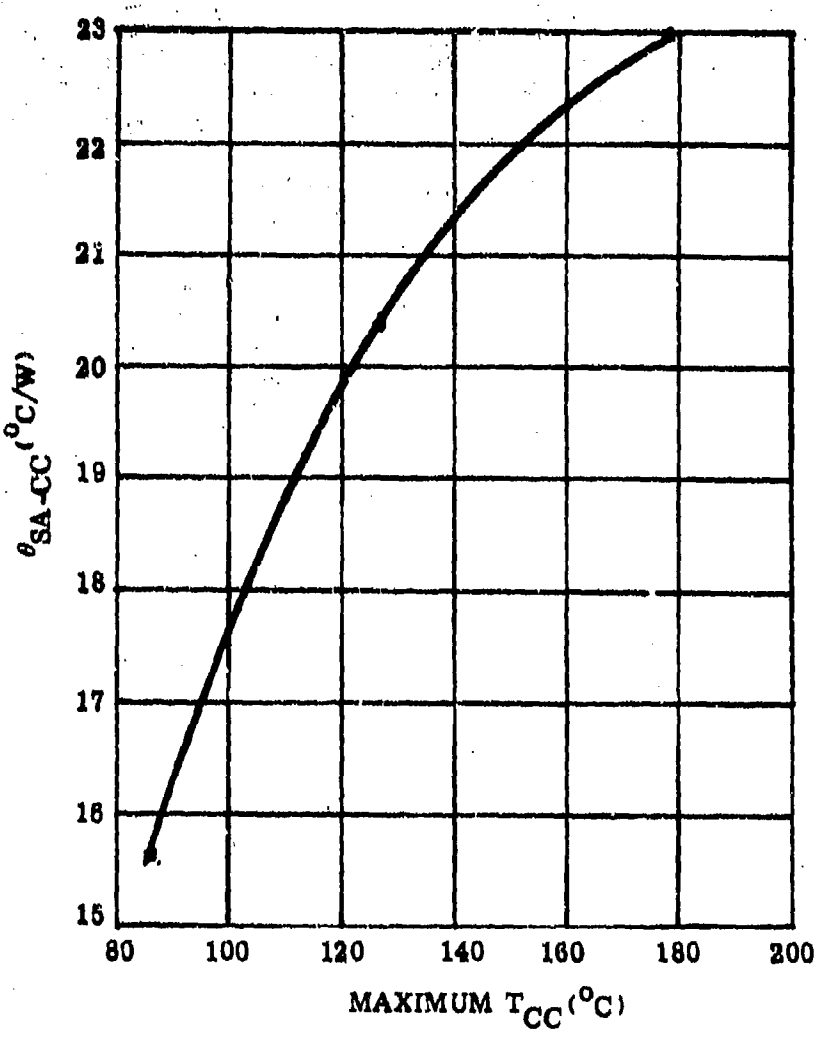


Figure 2.26 Comparison of Thermal Resistance as a Function of Maximum Chip Carrier Temperature

A precision sample-and-hold circuit samples the base-emitter voltage after a controllable delay. A second identical sample-and-hold samples the thermocouple probe voltage, which measures the chip carrier temperature. The measurement part of this fixture was used, in conjunction with the low-power fixture, to obtain the thermal cooling curve of an SCP 14 thermal test chip. A block diagram of the system is shown in Figure 2.27. The transistor under test has its emitter power current supplied through an isolating diode. A pulse generator (PG 1) applies negative pulses to the base of a PNP gate transistor, turning it on hard and diverting the emitter power current to ground, while the measurement current continues to be supplied. PG 1 also triggers a second pulse generator, PG2, which, after a controllable, variable delay, supplies a one μs pulse to the sample-and-hold circuits. This pulse is one μs wide, so the sample of voltage is an average over one μs.

The interval between the leading edge of the gating pulse and the sampling pulse is measured by an oscillator counter with a resolution of 0.1 μs and an accuracy of perhaps 0.3 μs. The gating pulse width and repetition rate are variable; in this experiment the repetition rate was 0.2 Hz.

The thermocouple probe output is amplified by a factor of 100 by an operational amplifier, which is sampled simultaneously with the base-emitter forward drop. The samples are displayed on digital voltmeters.

To perform the measurement, the delay of PG 2 is varied and both samples are recorded for each delay. The junction voltage is used to calculate the junction average temperature and the thermocouple voltage is used to measure chip-carrier temperature. Thus ΔT_{JA-CC} can be obtained at various times after the cessation of power to plot a cooling curve.

In our original experiments we were unable to measure junction average temperature at short times due to junction clearing effects. An SCP 14 thermal test chip was then calibrated for a measurement current of 200 μA to reduce the clearing time sufficiently to permit measurements down to about 2μs. The data obtained are plotted in Figures 2.28 and 2.29 on linear and log log scales, respectively. There is good reason to expect that, for short times after the interruption of power, the junction temperature will decrease linearly with the square root of time [6]. Such plots for these data were made but no linear region was found. This behavior is well verified in larger discrete devices such as power transistors. It arises from the step-function response of a physical body in which heat flow is predominant in one dimension, which is nearly the case for a large discrete device. Apparently the spreading, in the case of this integrated circuit, occurs sufficiently rapidly that this phenomenon does not occur. An inspection of the transient curve, for θ_{JA-CC} reveals that major transients are completed in the first 10μs. Data were obtained out to 10ms where the thermal resistance had decayed to less than 20% of its initial measured value. The effect of the multiple time constant behavior is clearly evident, with the decay for times greater than about 50μs being much less rapid due to the longer time response of the substrate and package. Data for the shorter times were taken by interrupting the power for only 200μs at the repetition frequency of 0.2 Hz. Points from 55 μs out to

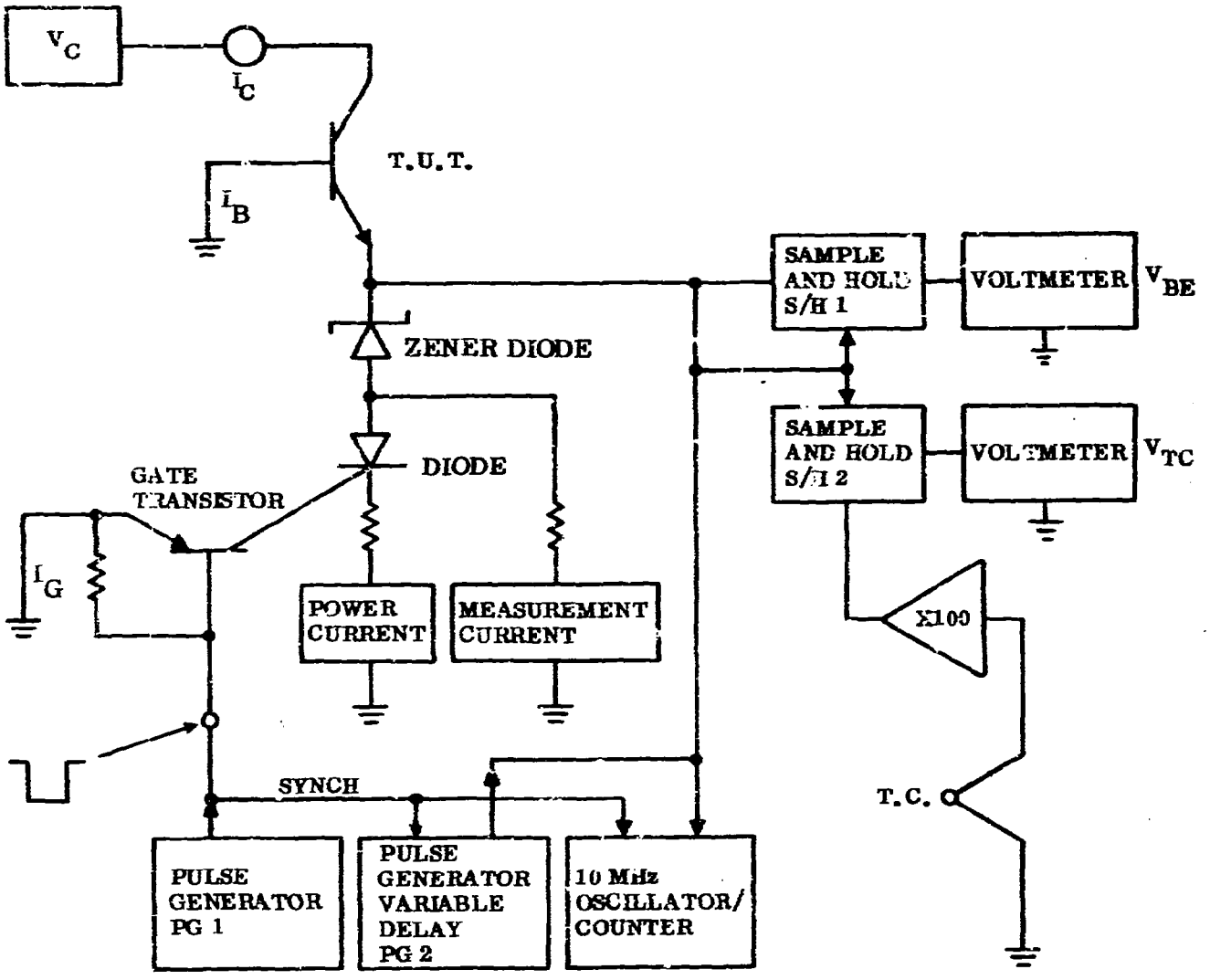


Figure 2.27 Transient Measurement Block Diagram

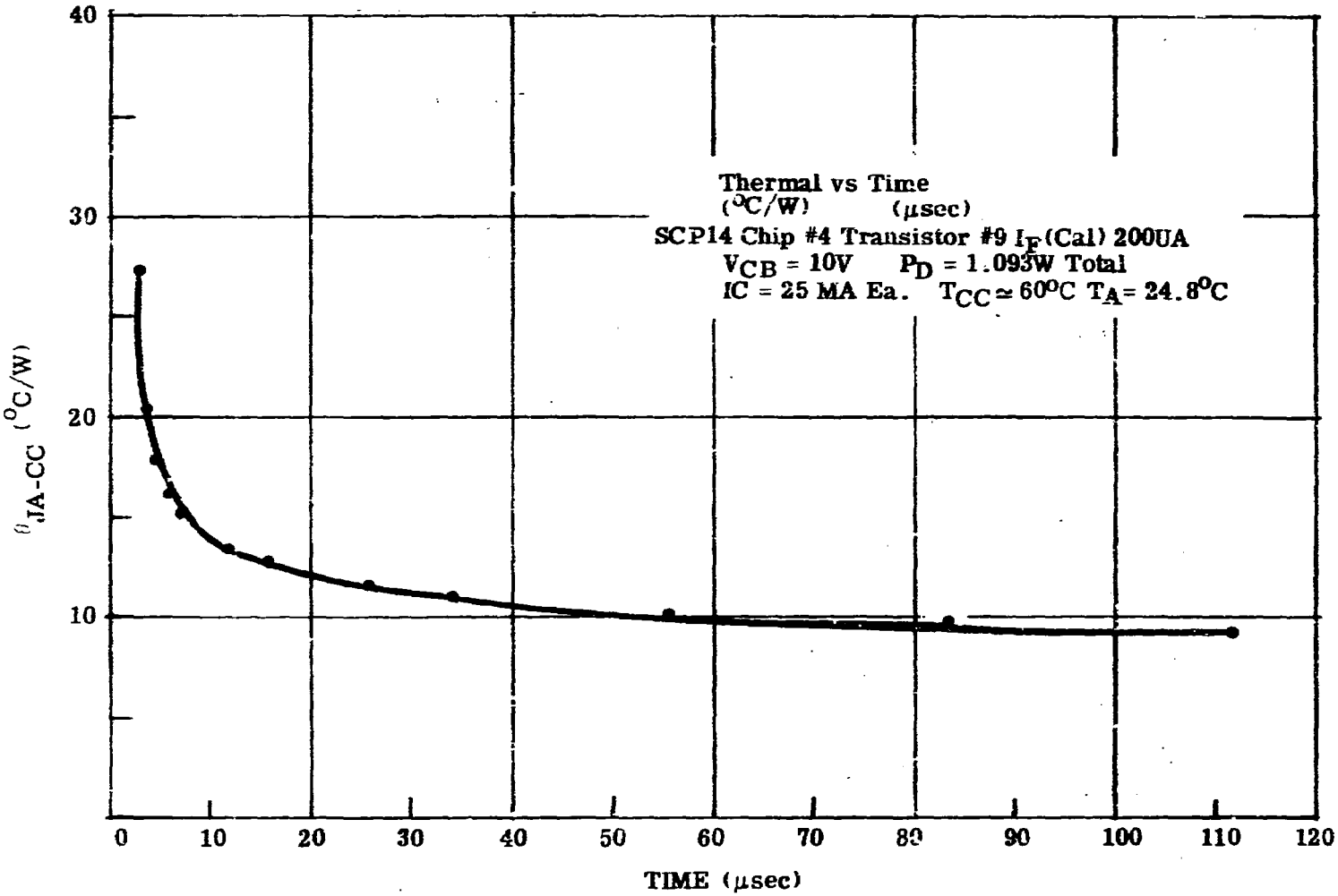


Figure 2.28 Transient Temperature Decay

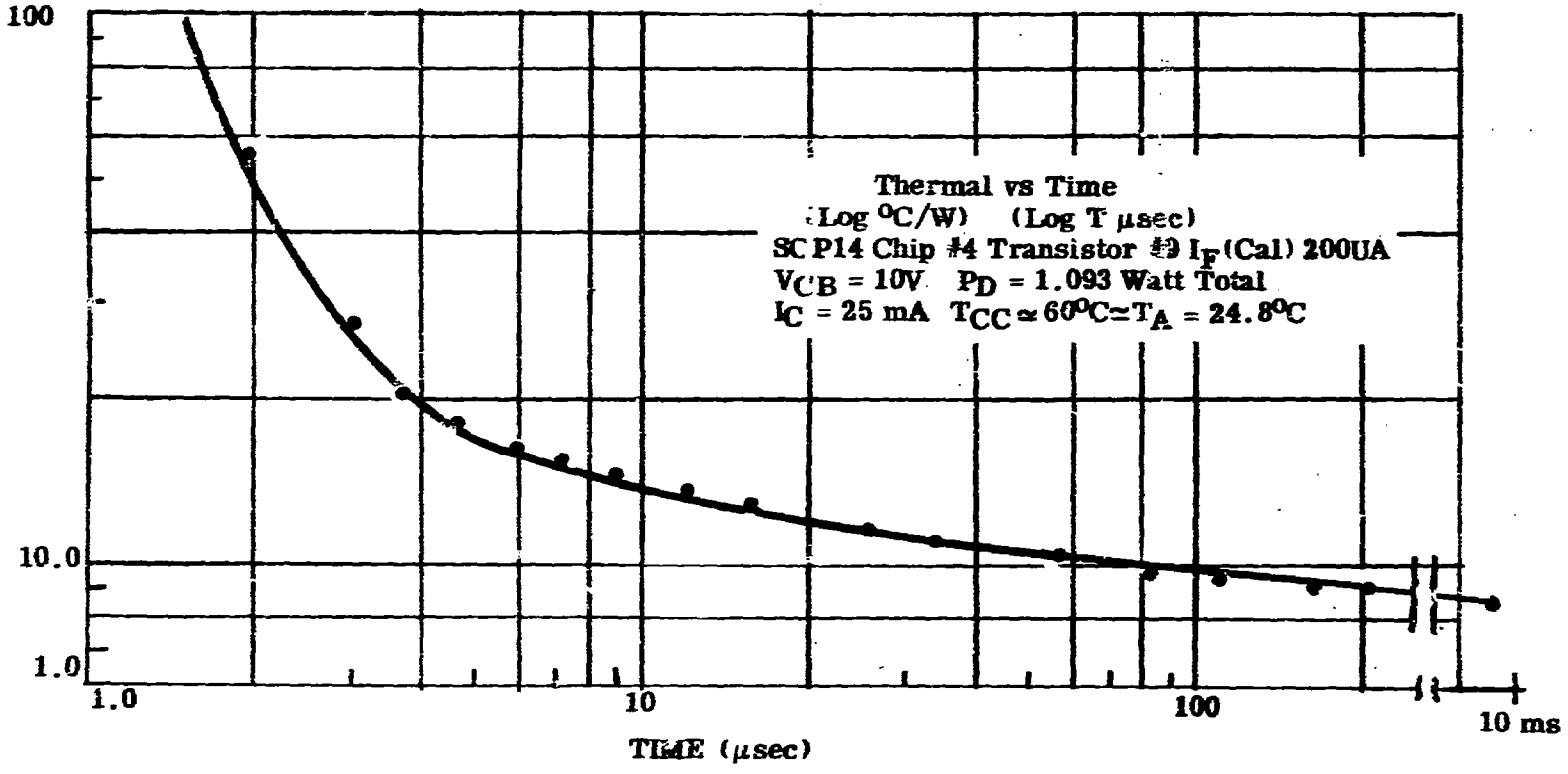


Figure 2.29 Transient Temperature Decay - Log-Log Plot

10ms were also measured with an interruption time of 12 ms. Figure 2.29 shows points at 1.5 μs and 2μs, demonstrating the continuity in the data. Caution must be observed in interpreting these points, however, since they surely infringe on the time when the junction is not yet cleared of stored charge, so that the temperature calibration cannot be relied upon. Observe that the point at 10ms falls one decade to the right of the margin of the graph.

2.2.5 DC - Pulsed Power Measurements

An experiment was performed to measure the effect of pulsed power on the measured thermal resistance. This was done by using the gating fixture described in section 2.2.4 on transient measurements. An SCP 14 test chip mounted in a D3 package was used for this test. A gating circuit was used to interrupt dc power to the chip (all four transistors) for various times, at a fixed frequency of 100 Hz. The interruption times were 1, 10, and 100 μs, and 1 and 5 ms, corresponding to duty cycles of 99.99%, 99.9%, 99%, 90%, and 50%. The value of applied power was calculated by measuring the fixed collector and base-emitter voltages during the power-on phase with an oscilloscope; currents were measured with a D'Arsonval meter whose response time was slow enough to measure average current. Since the current wave form was essentially rectangular the product of voltage and current gave the average power in the four transistors. The results of this experiment are shown in Table 2.2.

TABLE 2.2 Thermal Resistance Measured at End of Off-Time For Various Duty Cycles

OFF-TIME μSEC	DUTY CYCLE %	θ_{JA-CC}* $^{o}C/W_C$
1	99.99	16.7
10	99.9	16.2
100	99	15.4
1000	90	14.4
5000	50	14.3

* Based on average power dissipation over complete cycle.

2.2.6 Forced-Air Cooling

An experiment of the effect of forced-air cooling on a device, as a function of heat-sink temperature, was performed using an SCP-14 chip mounted in a D-3 package, and the 15x objective. The device was mounted on the heat sink and the thermal resistance was measured in still air and with a stream of room-temperature air flowing at 1000ft/min. over the open surface of the package. The results are summarized in Table 2.3.

TABLE 2.3 Thermal Resistance Values for Increasing Temperature With or Without a Forced Air Ambient

HEAT SINK Temperature (^oC)	STILL AIR AMBIENT $\theta_{JR-CC}(^oC/W_C)$	FORCED AIR AMBIENT θ_{JR-CC} $(^oC/W_C$
60	17.0	19
80	13.0	12.7
100	14.3	15.8
120	18.3	14.9

The anomalously high values, of thermal resistance at $T_{HS}=60^o$ were discovered to be due to a lack of proper contact of the probe at the time of the first trial. The difference in still air and forced air thermal resistance values at 80^oC and 100^oC are within the limits of experimental error. The effect of forced air at $T_{HS} = 120^oC$ appears to reduce the junction region-to-chip carrier thermal resistance. This effect is contrary to previous measurements and analysis [1]. Therefore these tests are subject to too great an experimental error to draw any valid conclusions.

2.2.7 I^2L Device Measurements

Integrated Injection Logic semiconductor microcircuits were not commercially available at the time this project was done. In order to make measurements on this type of device, 10 samples of a custom I^2L circuit, fabricated for research purposes at the General Electric Electronics Laboratory, were obtained and used for measurement. The devices were mounted in D1 packages. Hot spots of nearly identical temperature were found on the output transistors of these devices. The average of three measurements for each device is reported. The results for two devices are presented in Table 2.4. Some of the other devices were found to be faulty, and some were damaged in the process of coating them. Measurements were taken at a heat sink temperature of 60^oC and 100^oC with the 15x objective, with an applied power of about 0.4 watts.

TABLE 2.4 Thermal Resistance of I^2L Circuit in D1 DIP

SERIAL NO	$T_{HS} = 60^o$ θ_{JR-CC} $^oC/W_C$	$T_{HS} = 100^o$ HS θ_{JR-CC} $^oC/W_C$
4B	29.9	29.5
4D	30.3	29.9

There is no significant variation; there is no physical reason why these devices would be much different than more conventional devices in terms of thermal behavior, and it is seen that the measurements are quite comparable to those obtained on other devices.

2.3 COMPARISON OF COMPUTER SIMULATION AND EXPERIMENTAL RESULTS

2.3.1 Transient Temperature Decay

A computer simulation of the transient temperature decay was done and compared with the test measurements. The comparison is shown in Figure 2.30. An x-ray examination of the test package, shown in Figure 2.31, showed that solder voids in the chip bond could account for some differences as the values approached steady state. Reference [1] points out that the thermal resistance value can increase 3-5°C/W_C for a 55% solder void-about the same void extent as shown in Figure 2.31. The conclusion is that the results are not in very good agreement except for steady state results, which when corrected for the solder void effect, are in very good agreement.

For short time periods, $t < 10\,\mu$sec or so, the electrical transients in the chip measurement circuit are not settled out. Since the thermal time constant of the junction average temperature as predicted by the computer simulations, is only seven μsec, then it is apparent that the electrical switching technique cannot be used to predict an accurate value of the junction average temperature or of the thermal time constant.

2.3.2 Variation of Thermal Resistance with Power Input

Figure 2.32 compares the experimental results measured with an IR microscope (with a 74x objective lens) with the computer-simulation results. The experimental data have been reduced by using linear regression to obtain thermal resistance values and thus a straight line function is obtained. The experimental values are much lower than that predicted by the computer.

A number of things may be causing this difference between the measured and simulated result, but no definite cause can be suggested at this time. One possible explanation is that the "effective junction" area actually increases as the power is increased. Reference [7] states that, as power is increased in a semiconductor, there may be significant space charge that causes the distinction between the depletion and neutral regions to be wiped out resulting in effect, in a larger heat dissipation area. Another possible explanation is that the microscope actually integrates energy over a much larger area than is now assumed (three "spot size" diameters). Note, the curve for an equivalent diameter of 3.7 mils in Figure 2.32. This curve does have values that are, at least, in the approximate range of values of the measured data. Another possibility is that the glass coating is not as effective as predicted and the lower temperature ambient IR radiation is being reflected from the metallization into the objective lens, similar to the effect suggested in reference [1]. Another possible cause for the difference might be in the experimental techniques. For example, the thermal probe measurement for T_{CC} was not as accurate as expected. Linear regression of the experimental data indicated, in general, that the thermal probe had a lower temperature (about 5-6°C) than that of the chip carrier. This difference is much greater than that found by the same technique in the previous study [1]. A possible explanation is that new probes were made up and different persons made the measurements for this current study. Another possible explanation is that the computer simulations may not be as accurate as anticipated. However, the same models were used, with some minor changes, in the current study as for the previous study. All of these explanations could

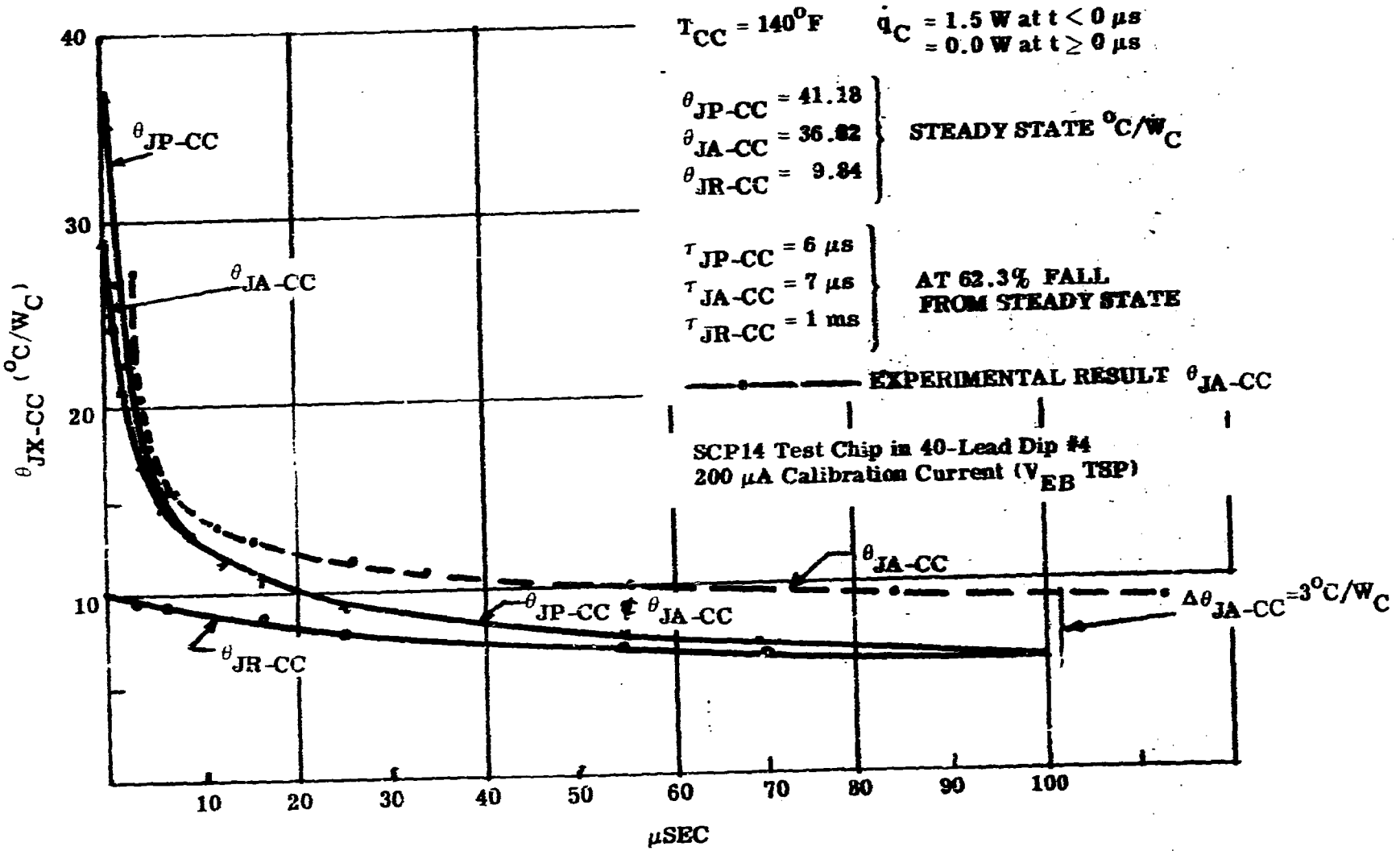


Figure 2.30 Transient Temperature Decay of SCP14 Test Chip

Figure 2.31 Chip with Solder Void

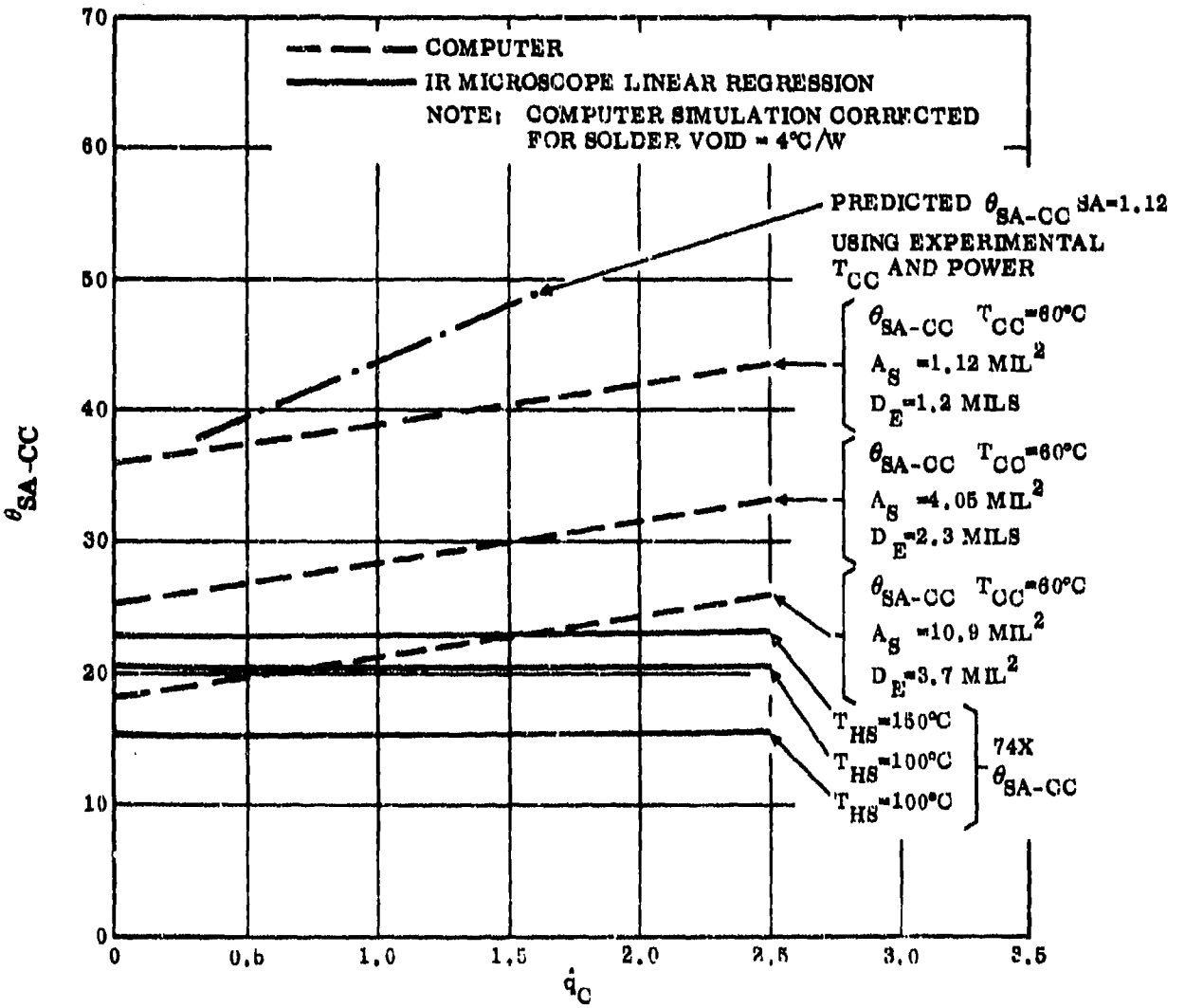


Figure 2.32 Comparison of Thermal Resistance with Power Between Computer Results and Experimental Results

account, in part, for the differences found.

2.4 Recommendations

The difference between the computer simulated results and the experimental results should be studied further to obtain a more accurate correlation between these results.

3.0 HIGH TEMPERATURE THERMAL CHARACTERISTICS

3.1 COMPUTER-AIDED SIMULATION AND ANALYSIS

3.1.1 General

The purpose of this portion of the study was to predict junction peak, junction average, and junction region thermal resistances at elevated chip carrier temperatures. This was done by varying the chip carrier temperature in the thermal chip and junction region models described in Section 1.3. In both models, temperature-dependent material properties are taken into account as the values of junction peak temperature, junction average temperature and junction region temperature are computed. These same models were used to predict the thermal time constants ($\tau_{X\text{-}CC}$) for the various values of T_{CC}.

3.1.2 Thermal Characteristics

The input parameters for the computer simulation included a power dissipation in the chip of q_C = 1.5 watts, distributed symmetrically to four junctions with 0.375 watts each. A heat sink temperature, simulated at 66°, 150°, 200° and 250°, resulted in chip carrier temperatures of T_{CC} = 70°, 156°, 206°, and 257°C, respectively. The results of the simulations are shown in Table 3.1, which lists the data obtained from the chip and junction region models, and shows the temperatures obtained by superimposing the data. It also lists the thermal resistance values calculated from the relationship

$$\theta_{XX\text{-}CC} = \frac{T_{XX} - T_{CC}}{q_C} .$$

These thermal resistance values were then used to plot the data shown in Figure 3.1, which shows the variation of thermal resistance as a function of temperature. To provide an insight into the way the temperature is distributed within the junction region and chip, isothermal plots were constructed for each chip carrier temperature and are shown in Figures 3.2 through 3.5. It can be seen that there is a three-dimensional heat flow and, thus, spreading resistance, from the junction to the chip carrier. This spreading resistance depends on the geometry, power dissipation and, as shown in this report, the temperature and material properties of the chip and chip carrier.

In addition to the steady-state simulations, transient response curves were also simulated for T_{CC} = 70, 156 and 257°C. Figure 3.6 shows the results of the simulations and also lists the relative time constants obtained by reading the time at which each curve reached 63.2% of its steady state value. In order to compare this data with the IR experimental measurements, Figure 3.7 was constructed. The figure compares $\theta_{SA\text{-}CC}$ with T_{CC} for various surface areas. As in Section 2.1, the areas were normalized using the relationship

$$D_e = \sqrt{4A_S/\pi}$$

and the ranges of measurements (see description of range concept in Section 2.1) are as shown.

TABLE 3.1. Comparison of Thermal Characteristics for SCP 14 Thermal Test Chip at Various Chip Carrier Temperatures

	T_{HS}				Units
Chip Model Data	**66**	**150**	**200**	**250**	^{o}C
T_{JR}	66	178	233	288	^{o}C
T_{CC}	70	156	206	257	^{o}C
Junction Model Data					
ΔT_{JP-JR}	52	73	87	97	^{o}C
ΔT_{JA-JR}	45	63	75	84	^{o}C
Superimposed Temperature Data					
T_{JP}	138	251	320	385	^{o}C
T_{JA}	131	241	308	372	^{o}C
Effective θ Values Relative to Chip Carrier					
θ_{JP-CC}	45	64	76	85	$^{o}C/W_C$
θ_{JA-CC}	41	57	68	76	$^{o}C/W_C$
θ_{JR-CC}	11	15	18	20	$^{o}C/W_C$

Subscripts: J = Junction, C = Chip, P = Peak, A = Average, R = Region, HS = Heat Sink, CC = Chip Carrier

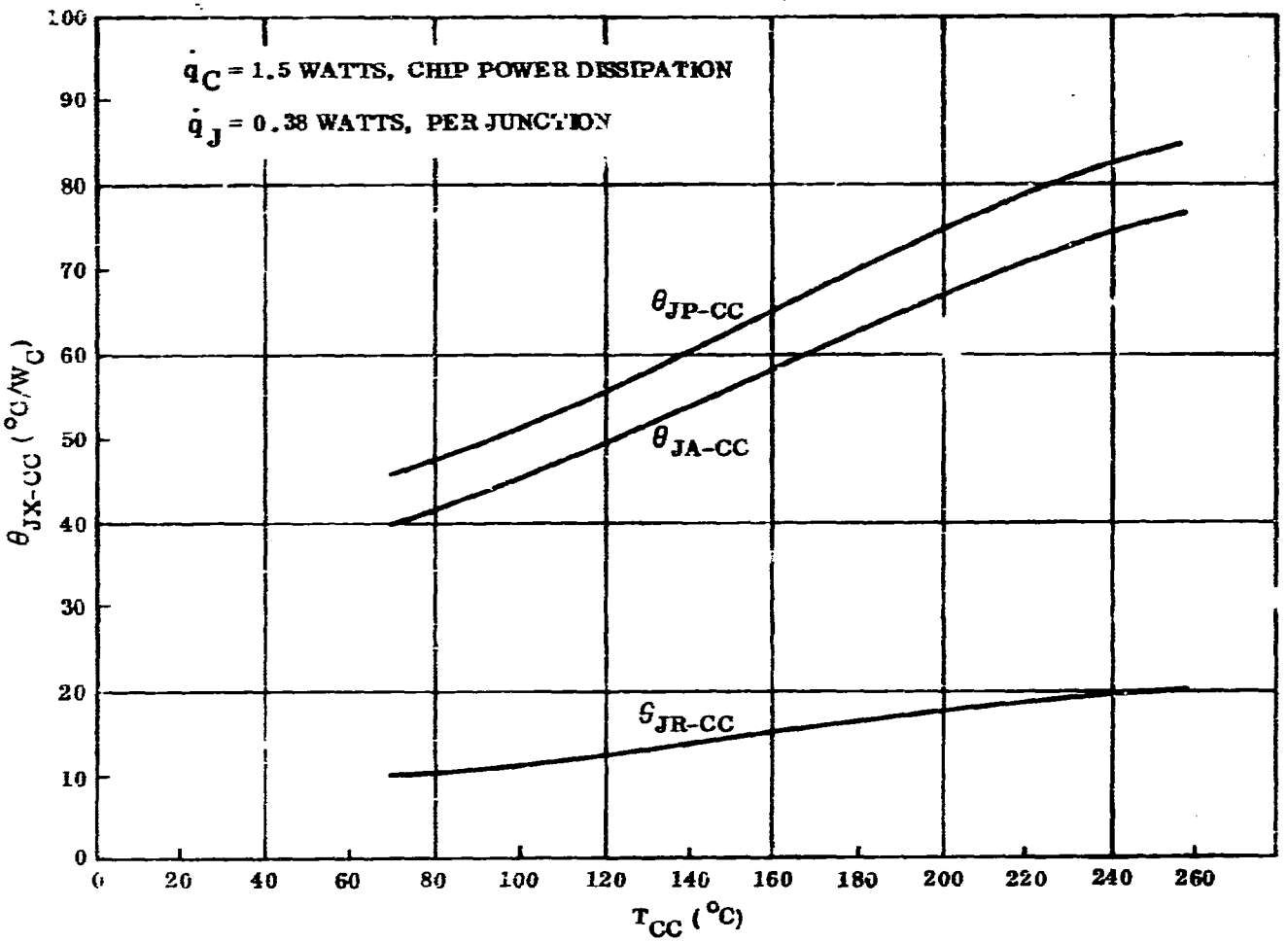


Figure 3.1 Comparison of Thermal Resistance Values as a Function of Chip-Carrier Temperature

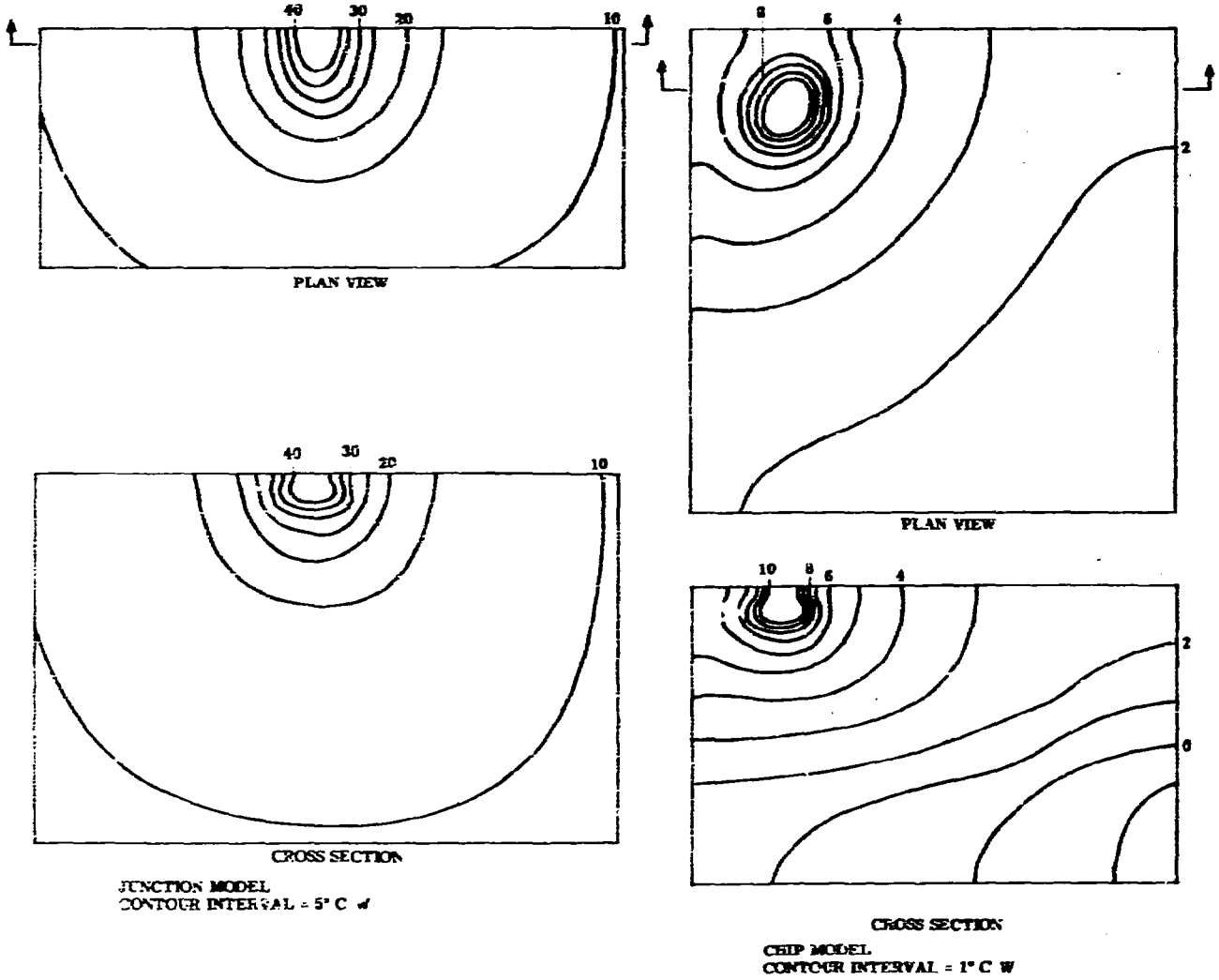


Figure 3.2 Isothermal Plots, $T_{CC} = 70^{o}C$, $\dot{q}_C = 1.5$ Watts

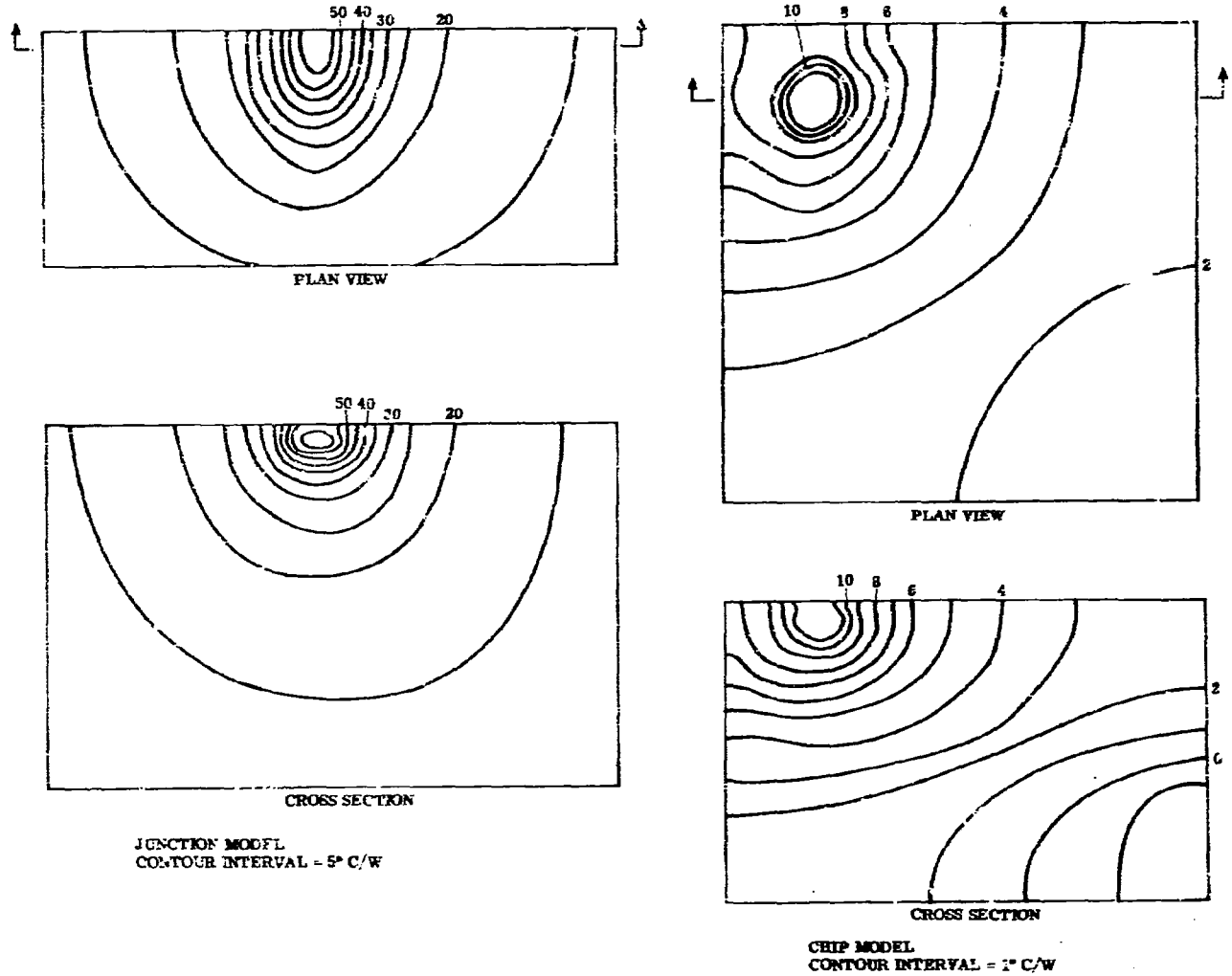


Figure 3.3 Isothermal Plots, T_{CC} = 56°C, $\dot{q}_C$ = 1.5 Watts

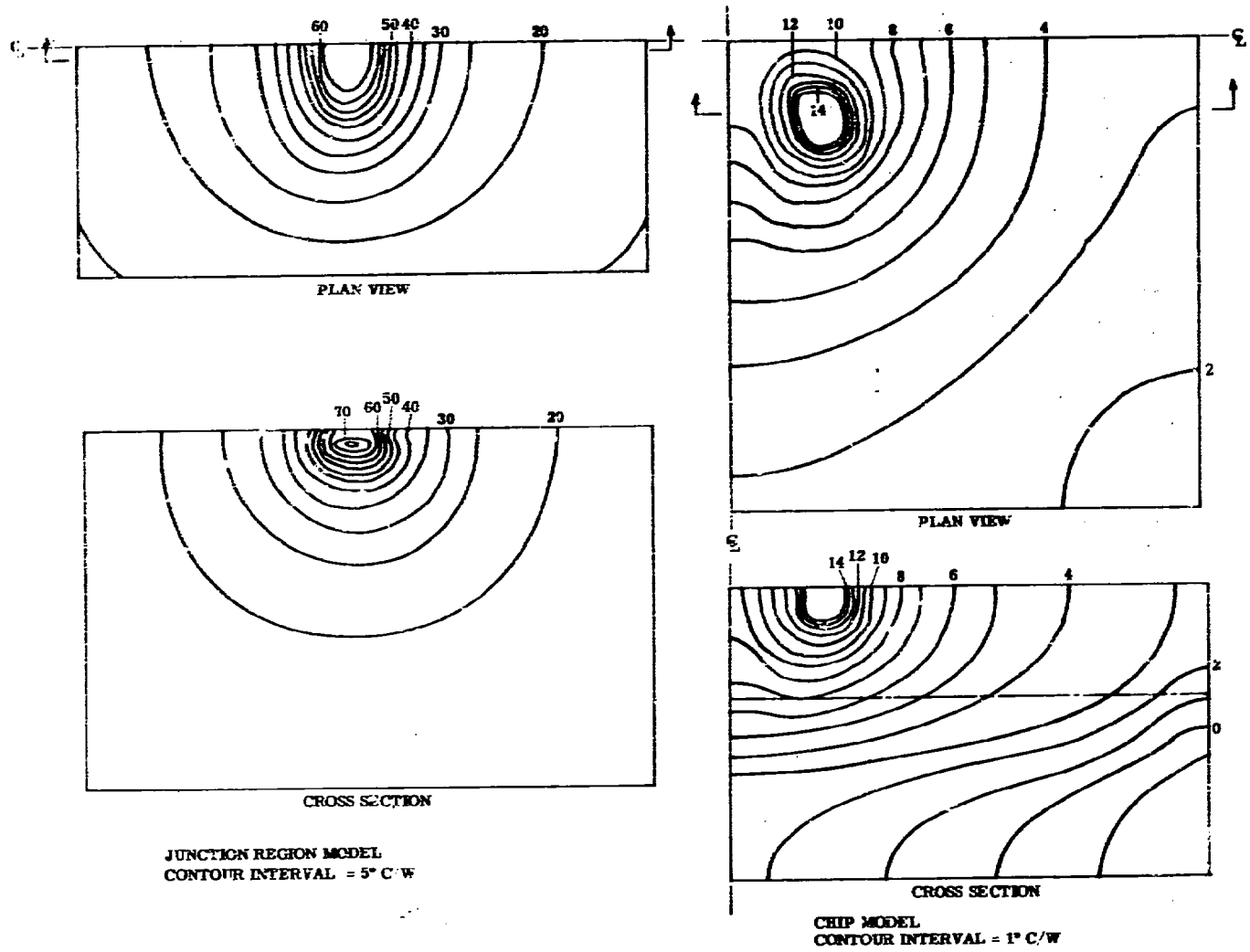


Figure 3.4 Isothermal Plot, $T_{CC} = 206^{\circ}C$, $q_C = 1.5$ Watts

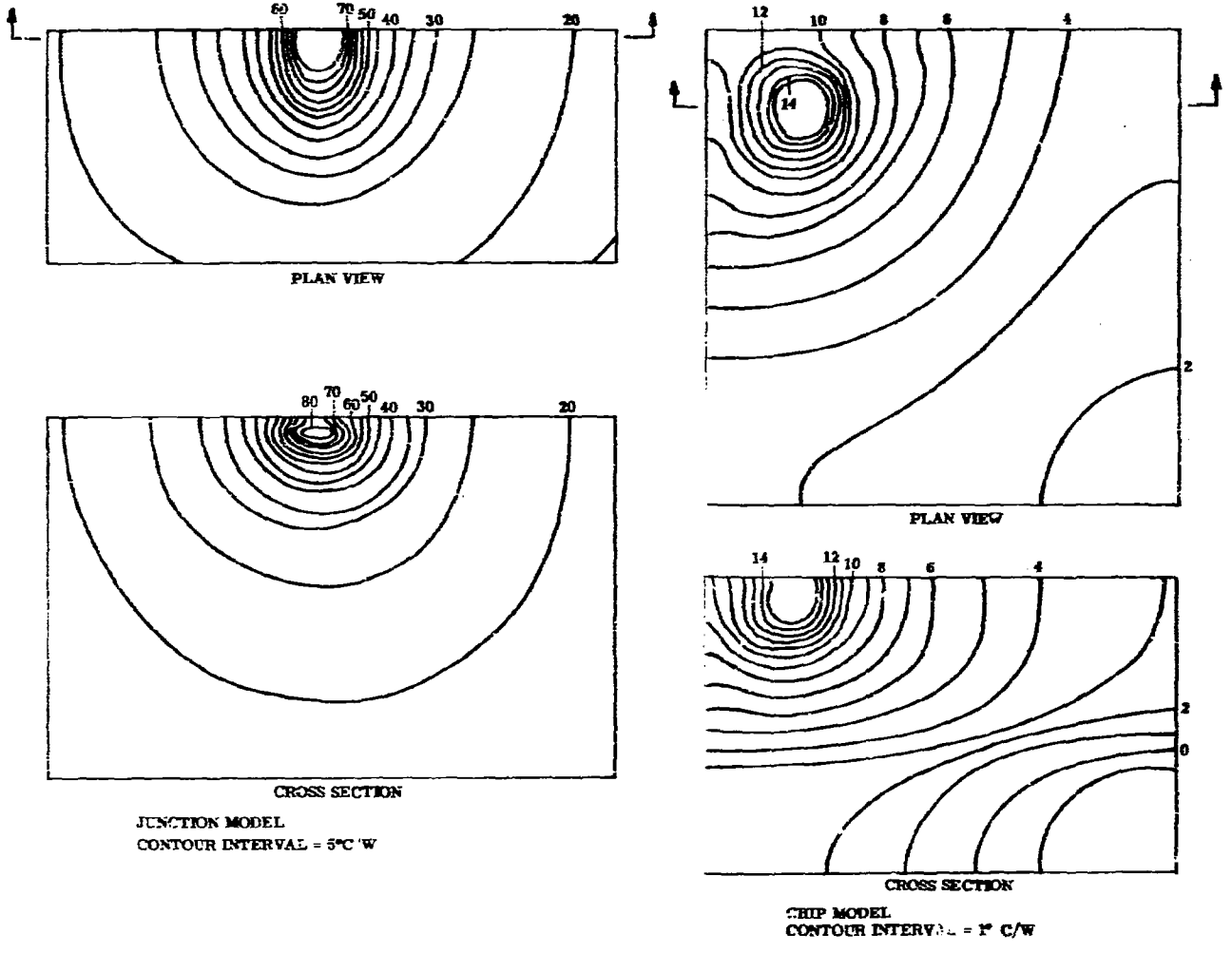


Figure 3.5 Isothermai Plots, $T_{CC} = 257^{o}C$, $\dot{q}_{C} = 1.5$ Watts

3.1.3 Theoretical Conclusions

3.1.3.1 Thermal Resistance Values

The results indicate that the thermal resistance, junction peak-to-chip carrier ($\theta_{JP\text{-}CC}$), increases at the rate of about $(\Delta\theta/\Delta T)_{JP\text{-}CC} = 0.2$ $(^{o}C/W)/^{o}C$ over the temperature range of $70^{o}C < T_{CC} \leq 260^{o}C$. This is the average slope of the curve for $\theta_{JP\text{-}CC}$ found in Figure 3.1. Thus, a $100^{o}C$ rise in T_{CC} will cause an increase in $\theta_{JP\text{-}CC}$ of about $20^{o}C/W_{C}$. For example, from Figure 3.1, $\theta_{JP\text{-}CC} \approx 53^{o}C/W$ at $T_{CC} = 100^{o}$ and at $T_{CC} = 200^{o}C$, $\theta_{JP\text{-}CC} \approx 75^{o}C/W$, which gives a $\Delta\theta$ of $22^{o}C/W_{C}$.

Correspondingly, the thermal resistance, junction average-to-chip carrier, and junction region-to-chip carrier, increases at an average rate of $(\Delta\theta/\Delta T)_{JA\text{-}CC} = 0.2$ $(^{o}C/W)/^{o}C$, and $(\Delta\theta/\Delta T)_{JR\text{-}CC} = 0.1$ $(^{o}C/W)/^{o}C$ respectively, over the same temperature range.

3.1.3.2 Thermal Time Constant

The thermal time constants increase with temperature. For example, Figure 3.6 shows that the transient response of the junction peak temperature, relative to that of the chip carrier, is $\tau_{JP\text{-}CC} = 15$ μsec at $T_{CC} = 70\ ^{o}C$ while at $T_{CC} = 257\ ^{o}C$, the time constant is $\tau_{JP\text{-}CC} = 26$ μsec, an increase of about 70%. Similarly the thermal time constants for the junction average and junction region temperatures, relative to that of the chip carrier, have values of $\tau_{JA\text{-}CC} = 20$ μsec and $\tau_{JR\text{-}CC} = 1.8$ msec, respectively, at $T_{CC} = 70\ ^{o}C$ and they both increase by about 60% at $T_{CC} = 257\ ^{o}C$. An approximation of the relative thermal time constants at other temperatures, between $70\ ^{o}C \leq T_{CC} \leq 260\ ^{o}C$, can be obtained by interpolating between the tabulated data or the thermal response curves given in Figure 3.6. For example, to approximate the relative time constant $\tau_{JR\text{-}CC}$ at $T_{CC} = 200^{o}$, from Figure 3.6 $\tau_{JP\text{-}CC} = 19$ μsec at $156\ ^{o}C$ and $\tau_{JP\text{-}CC} = 26$ μsec at $T_{CC} = 257\ ^{o}C$; therefore at $200\ ^{o}C$, by interpolation, $\tau_{JP\text{-}CC} = 22$ μsec.

3.3.3 Infrared Measurements

It can be shown that an IR microscope will not necessarily read peak temperature values; in fact, for different objective lenses there may be a significant range in values (Figure 3.7). For example at $T_{CC} = 160^{o}C$ the reading for a 15X lens could range from a peak of about $53^{o}C/W$ to a low of about 25^{o} C/W — quite a variation!

3.2 EXPERIMENTAL RESULTS

3.2.1 General Remarks

The purpose of these tests was to determine thermal characteristics of representative devices at elevated chip-carrier temperatures. This was done by elevating the heat sink temperature and then taking IR microscope readings.

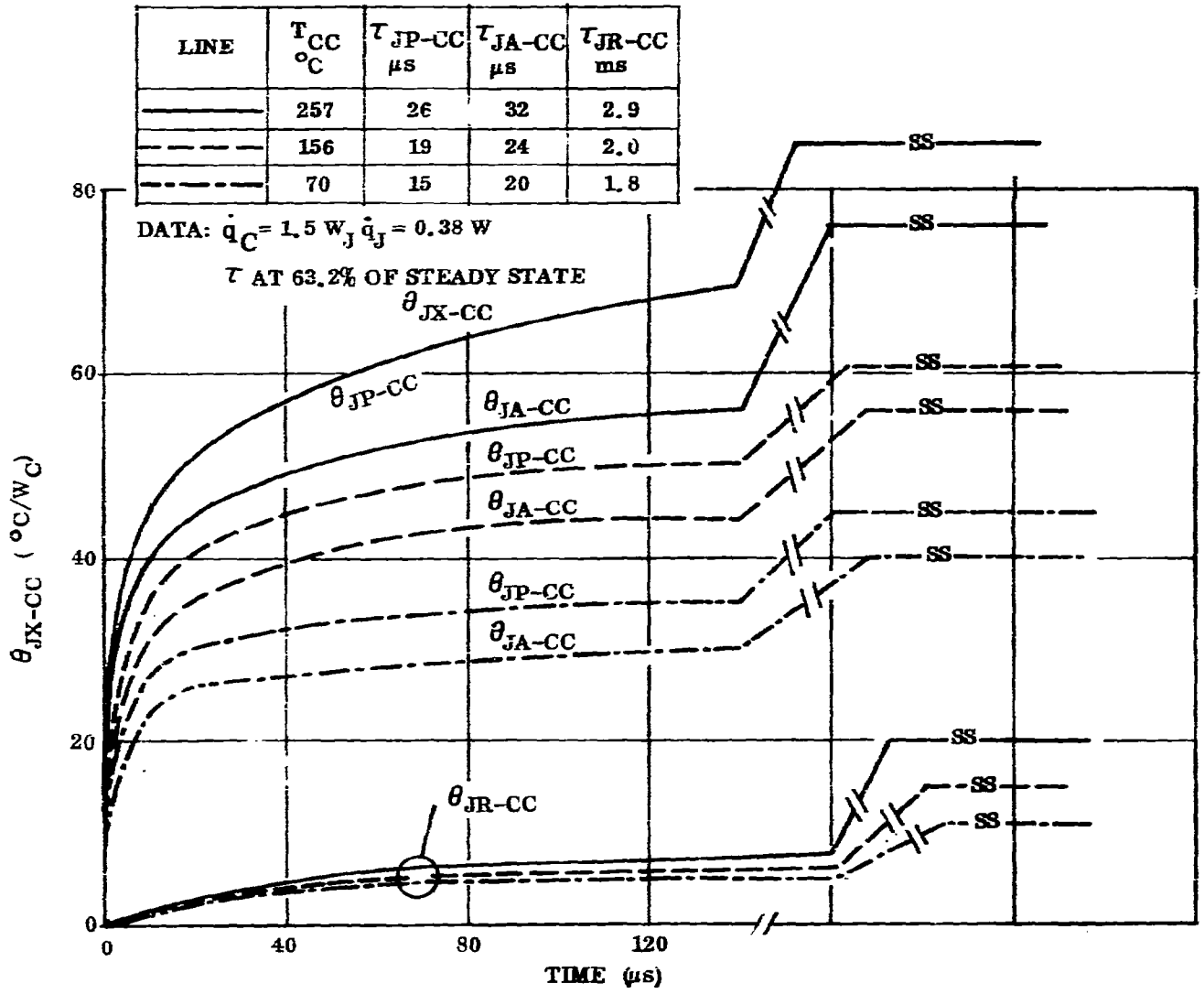


Figure 3.6 Transient Temperature Response Relative to Chip Carrier Temperature for Various Values of Chip-Carrier Temperature

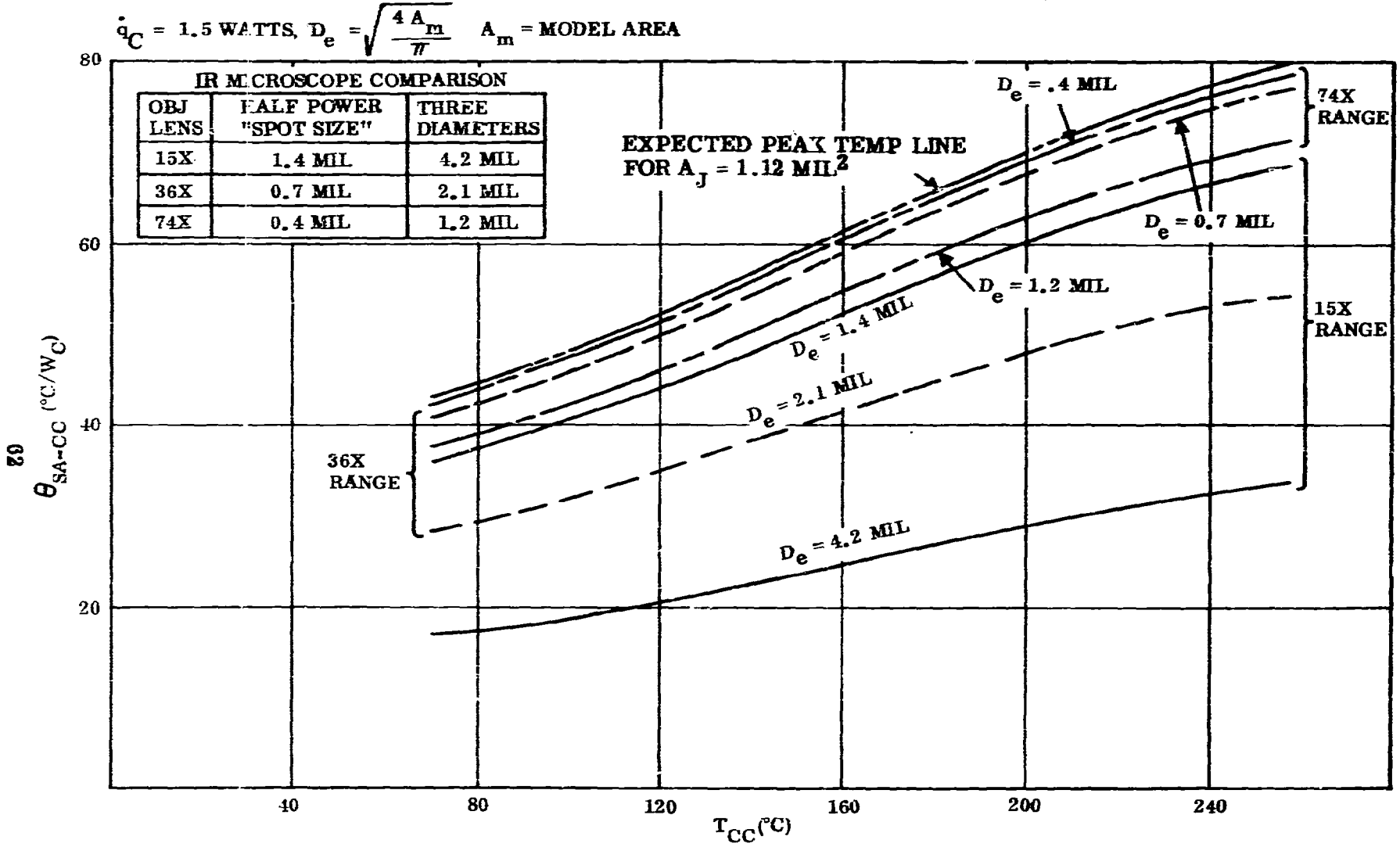


Figure 3.7 Comparison of Predicted θ_{SA-CC} Reading as a Function of Chip Carrier Temperature for IR Microscope Measurements

3.2.2 High Temperature Measurements

A series of measurements were made at elevated temperatures using the 15X objective on the IR radiometer. This lower-power objective was used because the short working distance of the higher-power objectives cause excessive heating of the housing, with possible danger of damage to the objective. Tests were made at heat-sink temperatures of 120° to 200°C. The highest junction temperature recorded was 290°C. A typical set of data is plotted in Figure 3.8 for a heat sink temperature of 160°C and various power dissipation rates. The results of several trials are plotted in Figure 3.9, with thermal resistance as ordinate and chip-carrier temperature as abscissa. These measurements are somewhat difficult and a smooth progression was not obtained. During the course of another trial at the highest temperature, the device failed, and the thermal resistance appeared to decrease, but the measurements were not repeatable. An examination of the transistor characteristics with a curve tracer showed that the transistor had become very leaky. The power applied was apparently being dissipated over a larger area due to junction breakdown and degradation, so that heat was no longer localized as before. Microscopic examination showed that the coating was severely cracked, and one lead was pulled away. The tests were discontinued at this temperature.

3.2.3 Effect of Power Level on $\theta_{SA\text{-}CC}$

The data of Figures 2.24 and 2.25 show that the power level has a negligible effect on the 15X IR measurement of $\theta_{SA\text{-}CC}$, provided only that the applied power level is sufficiently high to yield temperature rises large enough to be accurately measured, and that the level is not high enough to exhibit pronounced effects due to changes in thermal conductivity.

This implies that the temperature, which is controlled by heat-sinking and ambient temperature, is the variable that causes $\theta_{SA\text{-}CC}$ to vary. This is exemplified by the data presented in Figure 3.8 where each point was obtained by measuring $\theta_{SA\text{-}CC}$ for a range of applied power from about 300 mW to 1.5 W, with essentially constant $\theta_{SA\text{-}CC}$ over this power level group.

3.3 COMPARISON OF COMPUTER SIMULATION AND EXPERIMENTAL RESULTS

Figure 3.10 compares the computer-predicted thermal resistance values with the measured values obtained with the IR microscope using 74X and 15X lenses. The experimental results show a rising trend as T_{CC} increases, but the values are generally much lower than that predicted by the computer simulations. The reasons for the wide differences are not well understood and the possible explanations described in Section 2.3.2 also apply here. Note that the estimated curve for $\theta_{SA\text{-}CC}$ for $A_S = 10.9$ mils^2 ($D_e = 3.7$ mils) and the curve for $\theta_{JR\text{-}CC}$ fall within the experimental data, which correlates with some of the explanations found in Section 2.3.2. that dealt with the increase in junction size with power input, IR integration over a larger area, and the effectiveness of the glass coating but these curves still do not pinpoint the actual source of the differences. That will require further study.

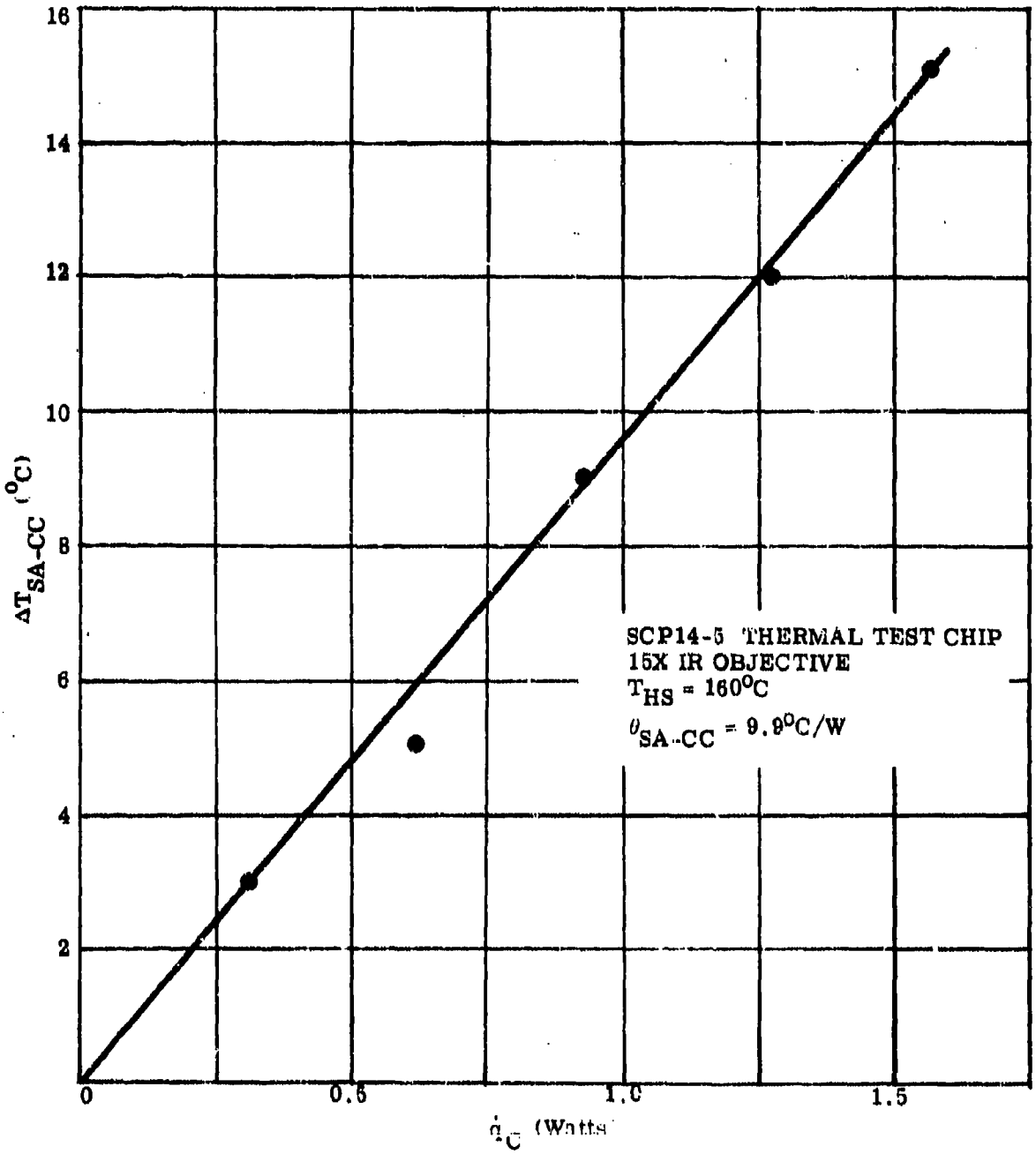


Figure 3.8 Typical Data Plot ΔT_{SA-CC} as a Function of Power Input

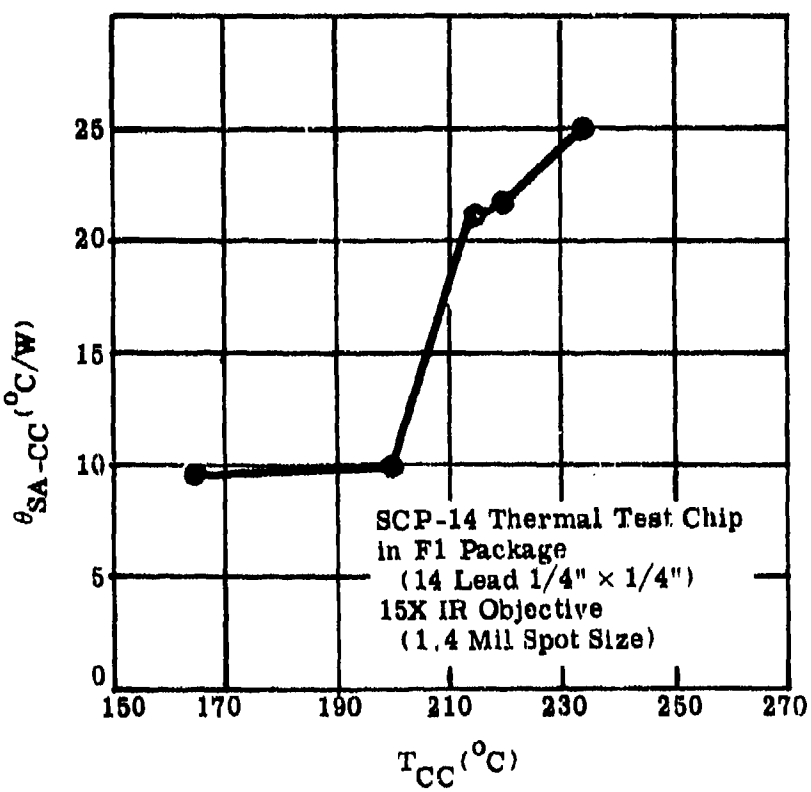


Figure 3.9 Variation of Thermal Resistance with Temperature

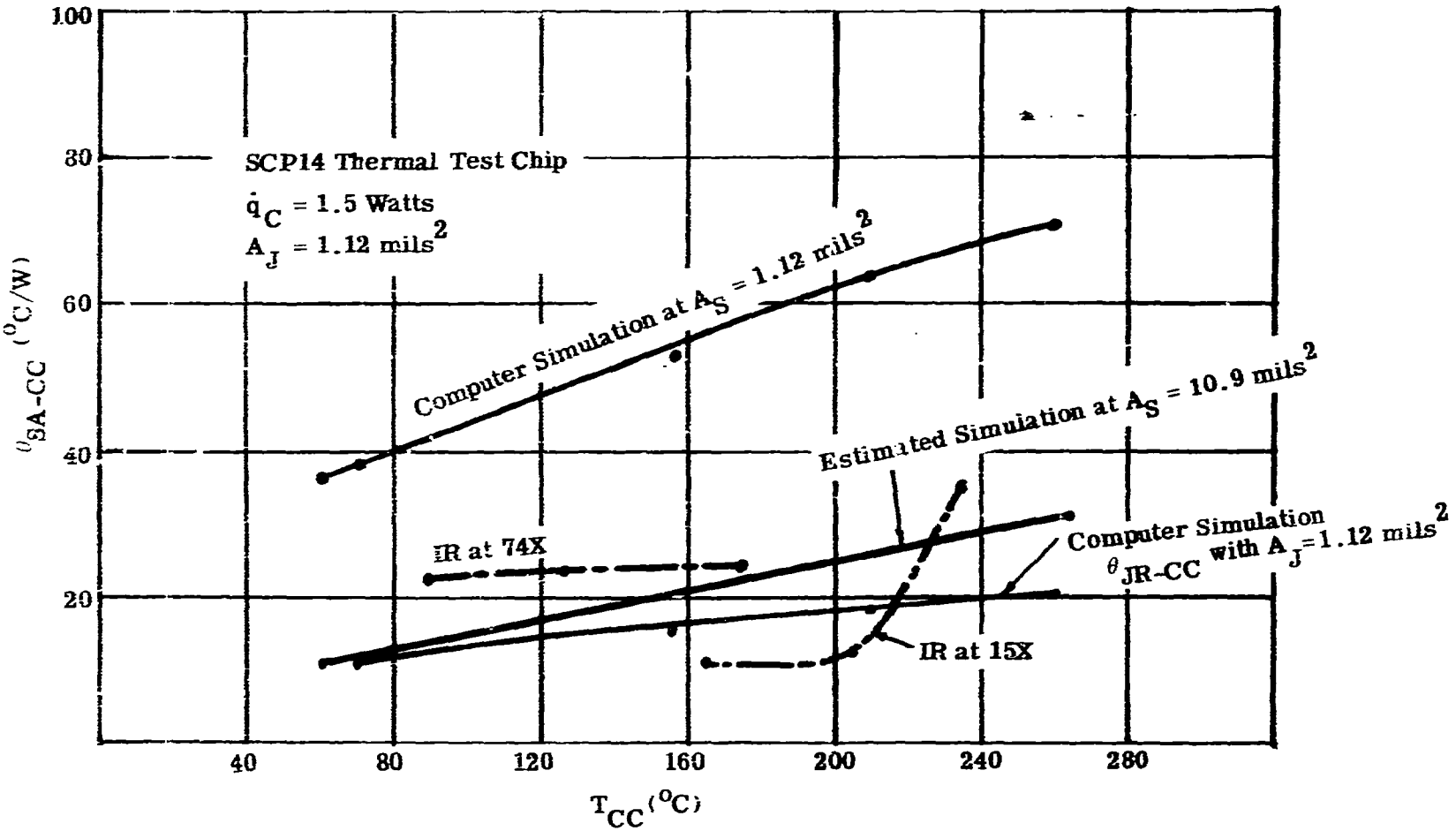


Figure 3.10 Comparison of Computer Simulation and Experimental Results

4.0 FILM CARRIER THERMAL CHARACTERISTICS

4.1 COMPUTER-AIDED SIMULATION AND ANALYSIS

4.1.1 General Remarks

The purpose of this portion of the study was to compare the thermal characteristics of the film carrier interconnection technique with that of wire-bonding. Toward this end two connection region models were developed, as shown in Figures 4.1 and 4.2. Geometry and materials for the Film Carrier model are based on data contained in References [8] through [11]; for the wire bond model the geometry and materials are based on data developed for the previous study, Reference [1] .

These models were used to determine the converging thermal resistance for heat flow from the chip through the connection lead, which was assumed to be 0.1" long. The SCP-14 Chip Model, described in Figure 1.4 was then modified by simulating this value of converging thermal resistance between the chip pads and the heat sink of those leads. As a basis for comparison the modified chip model was also run with no heat transfer through the leads (the converging thermal resistance value was set at infinity).

Two cases were run with the chip model for each interconnection technique; one case involved heat sinking through an alumina substrate; the other had heat sinking only through the leads. A comparison of these results is presented.

4.1.2 Results

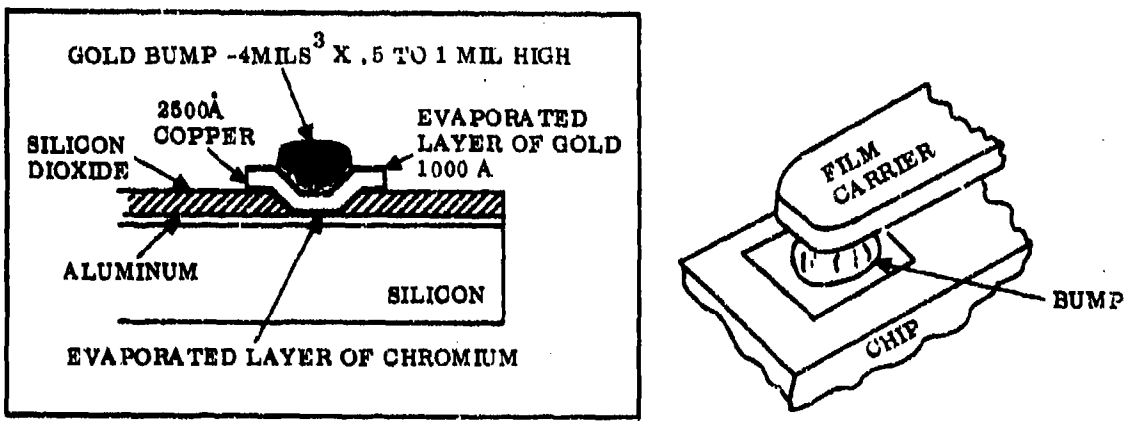
4.1.2.1 Converging Thermal Resistance Through Leads (θ_{CR-CC})

This resistance value was calculated using the relationship,

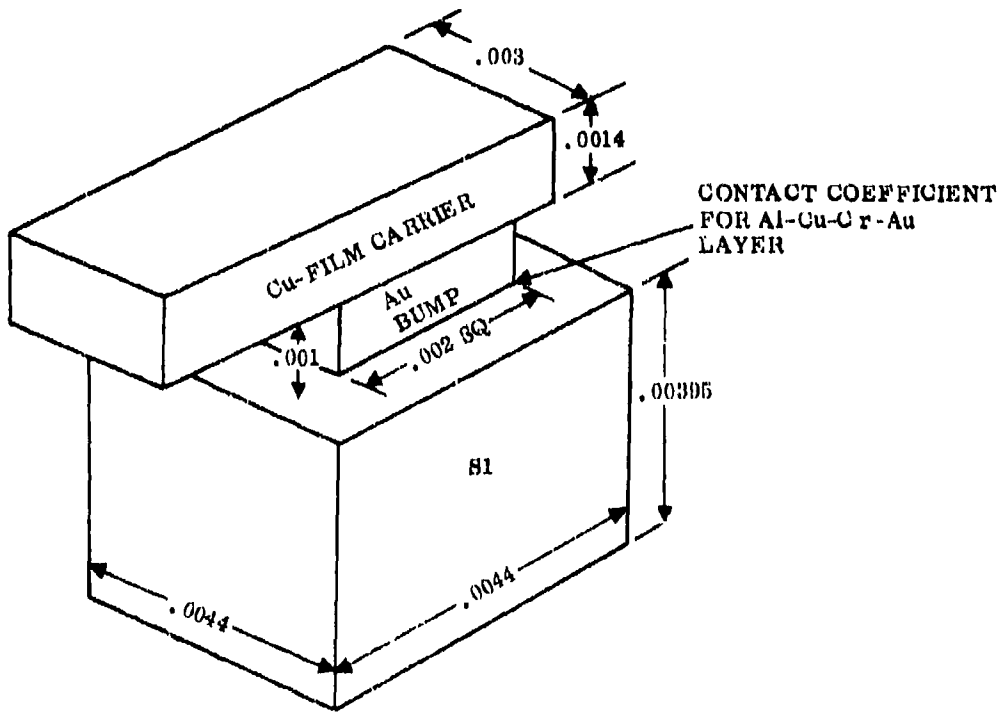
$$\theta_{CR-CC} = \frac{T_{CR} - T_{CC}}{\dot{q}_L} ,$$

where T_{CR} is the average temperature of the silicon Connection Region of the model,

T_{CC} is the assumed chip-carrier temperature, and $\dot{q}_L$ is the heat flow through the lead.

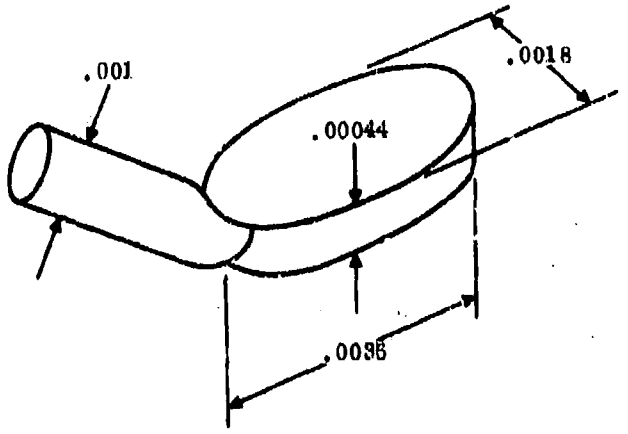


PHYSICAL MODEL

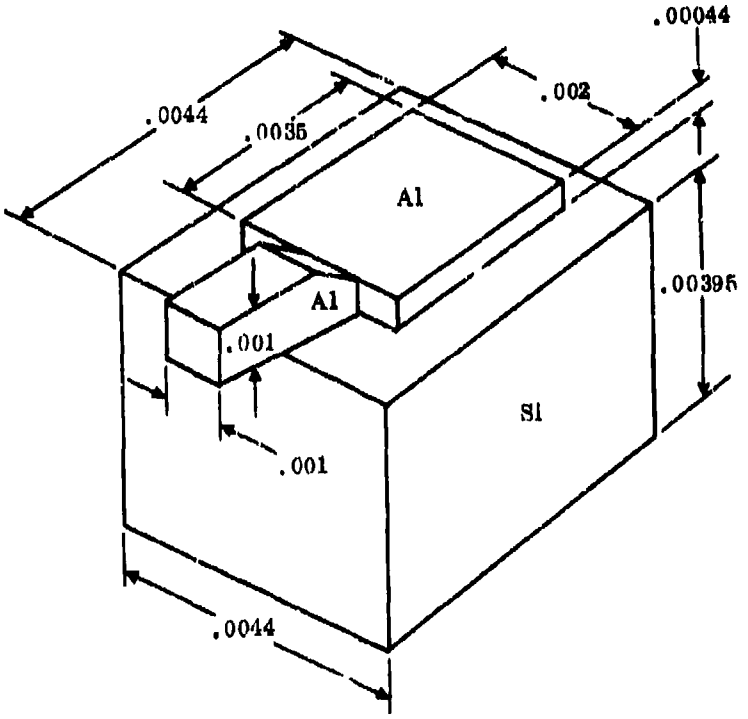


MATHEMATICAL MODEL

Figure 4.1 Physical and Mathematical Model of Film Carrier Connection Region



PHYSICAL MODEL



MATHEMATICAL MODEL

Figure 4.2 Physical and Mathematical Model of Wire Bond Connection Region

For the film carrier connection region model, shown in Figure 4.1, with $T_{CC} = 60^{\circ}C$ and $\dot{q}_L = .005$ watts, it was found that $T_{CR} = 72.6^{\circ}C$ which yields $\theta_{CR-CC} = 2526^{\circ}C/W_L$.

For the wire-bond connection region model, shown in Figure 4.2, with $T_{CC} = 60^{\circ}C$ and $\dot{q}_L = .002$ watts it was found that $T_{CR} = 93.4^{\circ}C$ which yields $\theta_{CR-CC} = 16678^{\circ}C/W_L$.

4.1.2.2 Thermal Resistance of Lead Per Unit Length, θ_L

Since θ_{CR-CC} was determined using a fixed 0.1" length of lead, the θ_{CR-CC} value was actually broken down into two series resistances, θ_L, the resistance of about 0.093" length of lead, and θ_{CR-L}, the resistance through the connection region, which also includes a small length of the lead itself. For the film carrier lead, the resistance was calculated to be $24.2(^{\circ}C/W_L)$/MIL and for the wire bond lead it was calculated to be $166.7(^{\circ}C/W_L)$/MIL. Then the resistance for the film carrier connection region was determined to be $\theta_{CR-L} = 267.2^{\circ}C/W_L$, and the resistance for the wire bond connection region was determined to be $\theta_{CR-L} = 1136.8^{\circ}C/W_L$.

4.1.2.3 Temperature Distribution Through Connection Region Model

The relative temperature distribution within each of the models can be seen in the isothermal plots of Figure 4.3, for the film carrier interconnection, and Figure 4.4 for the wire bond interconnection lead.

4.1.2.4 Thermal Characteristics of the SCP14 Chip Model with θ_{CR-CC} Added from Connection Region Models

The results obtained by the addition of the connection region model thermal resistances are summarized in Table 4.1. These results were obtained by adding a node to represent the connection region thermal resistance at each connection point (10 per model, 40 per chip) on the SCP14 Chip Model.

4.1.3 Theoretical Conclusions

It was found that the Film Carrier connection can dissipate about 7 times as much heat as a wire bond connection lead for a given allowable temperature rise. But, the film carrier still has a much higher thermal resistance than that through the chip to substrate bond. Therefore, a chip bonded to a substrate will have a much higher power dissipation capability by a factor of about 5:2, than one supported only by the leads. The addition of film carrier leads to a substrate mounted chip will produce about 1% decrease in the thermal resistance obtained without the leads (Table 4.1).

The thermal resistance of a chip without a substrate but with film carrier interconnections will be relatively high, but might be tolerable for low-power operation. Some improvement can be made in the film carrier values; however, the wire-bond values are pretty well fixed. For example, by doubling the thickness of the film carrier, the resistance, θ_{L-CC}, can be reduced about 50% since θ_{L-CC} is proportional to $1/A_{Lead}$. Substituting this value in previous calculations it can be shown that θ_{JR-CC} can be reduced from $74^{\circ}C/W_C$ to about $46^{\circ}C/W_C$ for a chip mounted with film carrier leads only.

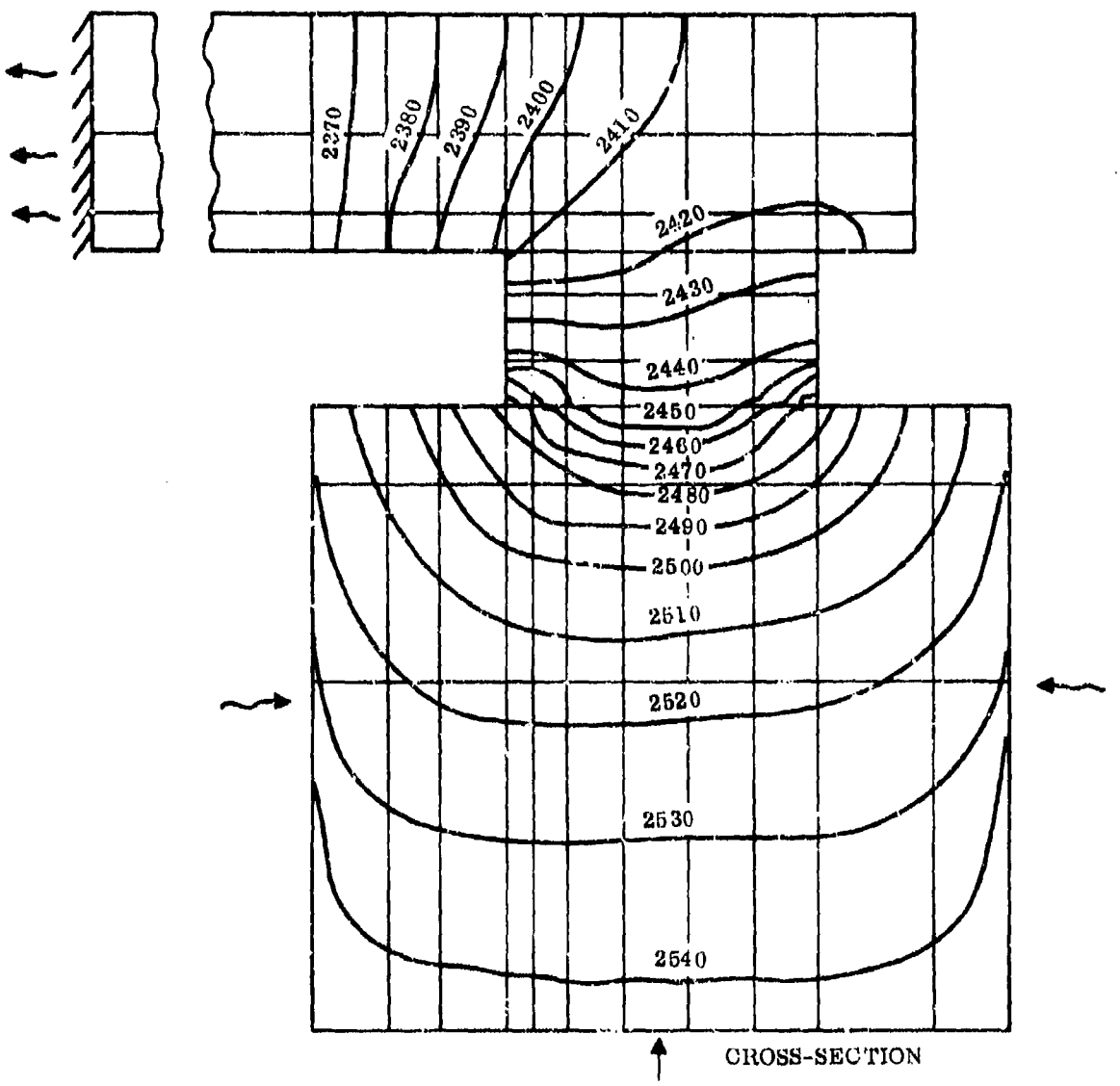


Figure 4.3. SCP14 Film Carrier Connection Model Isothermal Plot, Contour Interval = $10^{\circ}C/W_L$, $T_{CC} = 60^{\circ}C$, $q_L = 0.005$ Watts.

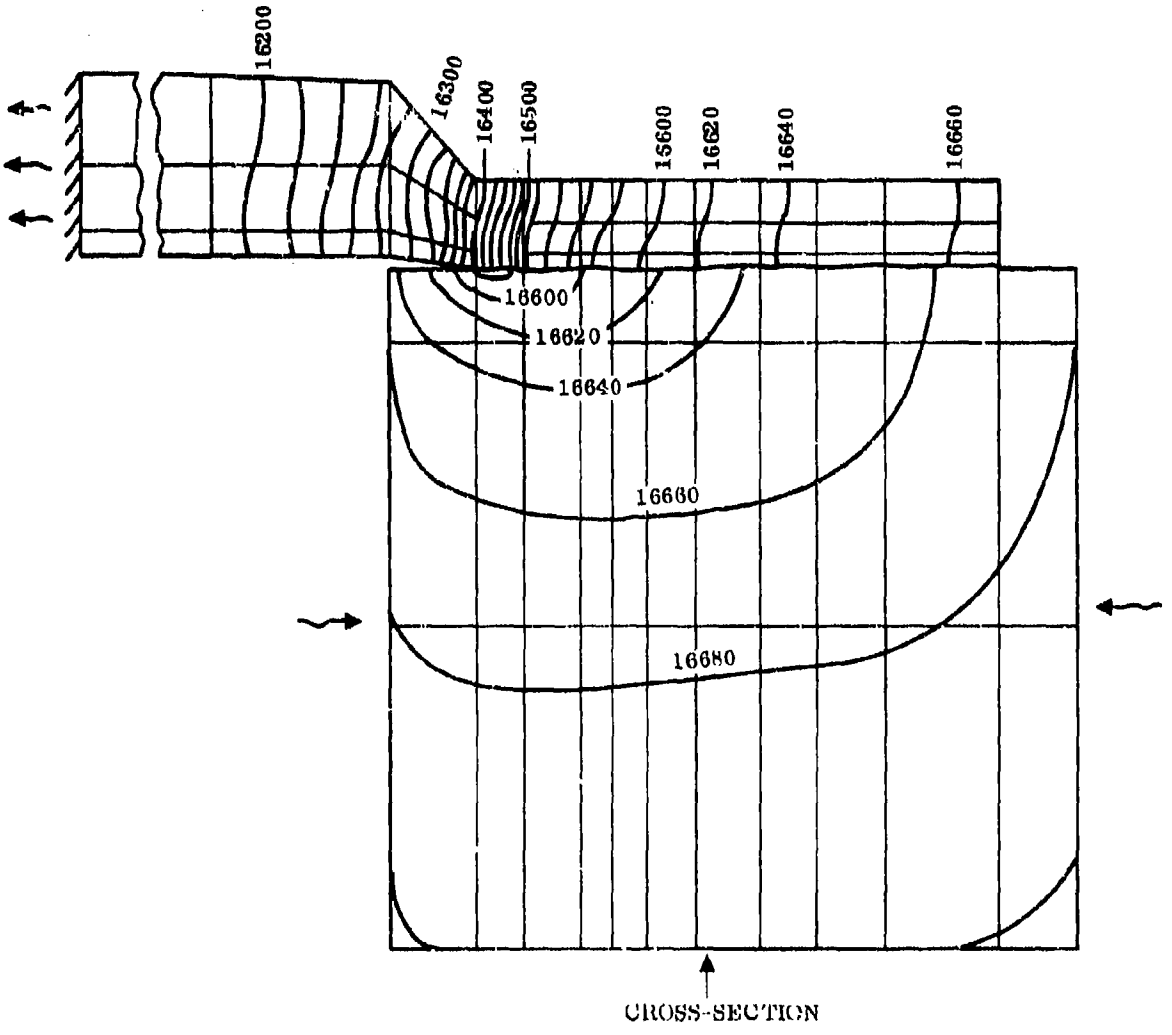
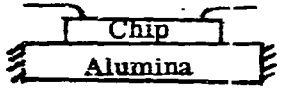


Figure 4.4. SCP14 Wire Bond Connection Model Isothermal Plot, Contour Interval = 20°C / W_L. T_{CC} = 60°C, q_L = 0.002 Watts.

TABLE 4.1. COMPARISON OF THERMAL CHARACTERISTICS BETWEEN FILM CARRIER AND WIRE BOND CONNECTIONS

PICTORIAL DESCRIPTION	θ_{JP-CC} °C/W$_C$	θ_{JA-CC} °C/W$_C$	θ_{JR-CC} °C/W$_C$	NOTES
	464	459	429	Wire bond leads (0.1" long) heat sunk to chip carrier $\dot{q}_C$ = .08 watts, T_{CC} = 60°C
	109	104	74	Film carrier leads (0.1" long) heat sunk to chip carrier $\dot{q}_C$ = .2 watts, T_{CC} = 60°C
	45.3	40.4	10.4	No heat transfer through leads substrate added $\dot{q}_C$ = 1.5 watts, T_{CC} = 70°C
	45.2	40.3	10.3	Wire bond leads heat sunk to chip carrier $\dot{q}_C$ = 1.5 watts, T_{CC} = 70°C
	45.0	40.1	10.1	Film carrier leads heat sunk to chip carrier $\dot{q}_C$ = 1.5 watts, T_{CC} = 70°C

It can also be seen that the film carrier has a fairly uniform temperature gradient and will therefore produce lower thermal stresses than the wire bond (see Figures 4.3 and 4.4). The thermal stresses will be especially high in the wire bond at the point where the bond transitions into wire in Figure 4.4.

4.2 EXPERIMENTAL MEASUREMENTS

4.2.1 General Remarks

The purpose of this portion of the study was to thermally characterize film carrier devices furnished by RADC. This was done using the IR microscope and the set-up described in Section 1.

4.2.2 Film Carrier Devices

Five devices packaged with the film carrier technique were supplied by the Rome Air Development Center. These devices were MC 5405 BCB HEX Inverters manufactured by Motorola and packaged in D-1 ceramic packages, with fritted-on lids. The chip and an opened package are shown in Figures 4.5 and 4.6. Three of the devices were damaged when opening packages or on coating. Measurements were obtained on the same output transistors of each of the remaining devices at a heat sink temperature of 60°C with the 15x objective lens. The results are shown in Table 4.2.

TABLE 4.2. THERMAL RESISTANCE OF FILM CARRIER PACKAGES

DEVICE	$\theta_{JR\text{-}CC}$ (°C/W$_C$) WITH TRANSISTOR ON PIN					MEAN (°C/W$_C$)
	1	2	3	4	5	
1	33.2	28.0	35.5	35.0	-	32.9
2	35.5	28	32.5	33.2	31.5	32.1

On both devices, the transistor labelled "2" seems to run somewhat cooler. There is no large spread, and the two samples yield, essentially, similar results. It should be noted that these packages were fabricated using a film carrier technique for the chip - but, the lead frame was wire-bonded to the chip pad. Only the chip was bonded to the film carrier lead frame. Therefore an experimental evaluation could not be obtained for the heat sinking effect of the leads.

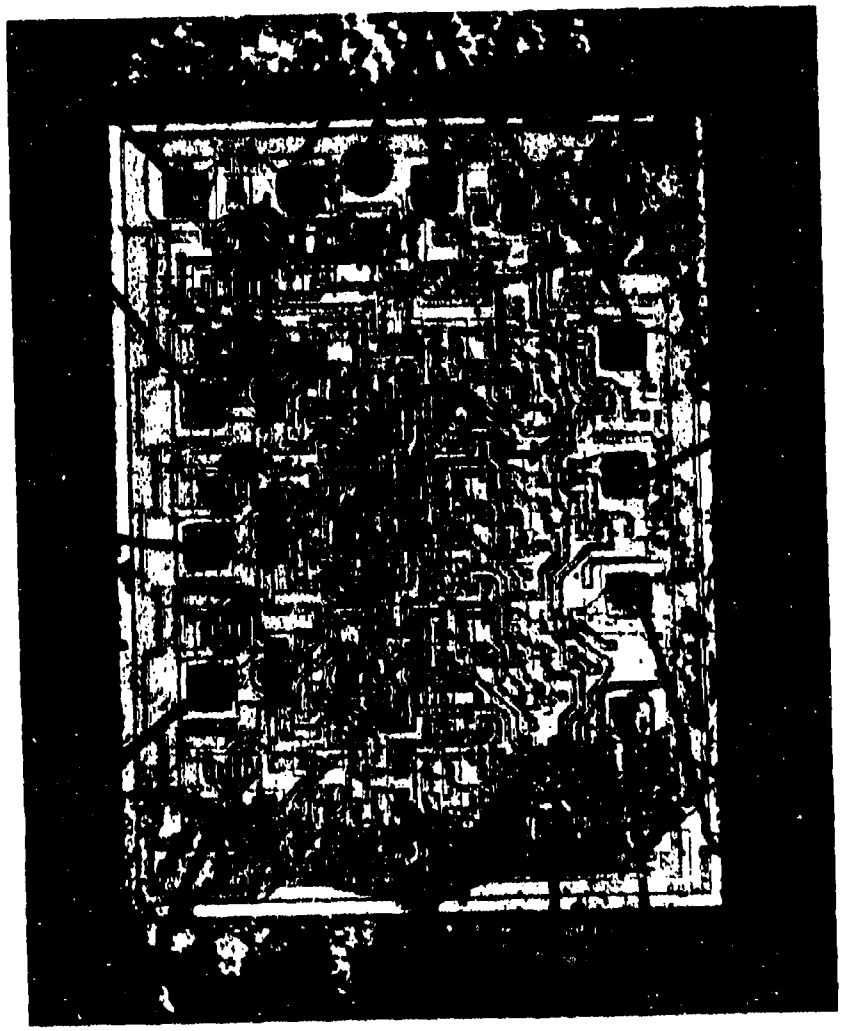


Figure 4.5 MC5404 Chip with Glass Coating

Figure 4.6. MC 5404 in D-1 Package.

REFERENCES

[1] G.K. Baxter and J.W. Brouillette, "Thermal Resistance of Microelectronic Packages", General Electric Company, Technical Information Series R75ELS027, May 1975.

[2] G.K. Baxter, "A New Recommended Method 1012 (Thermal Characteristics) for MIL-STD-883", General Electric Company, Technical Information Series, R75ELS026, May 1975.

[3] M.H. McLaughlin and N.D. Fitzroy, " Thermal Chip Evaluation of IC Packaging",IEEE Transactions on Parts, Hybrids, and Packaging, Volume PHP-8, No. 3, September 1972.

[4] Y.S. Touloukian, etal., Thermophysical Properties of Materials, Thermophysical Properties Research Center, Purdue University, Data Series: Plenum Publishing Corporation, 1970.

[5] J.E. Comeforo, "Properties of Ceramics for Electronic Applications", The Electronic Engineer, April 1967.

[6] M. Jakob, Heat Transfer, Vol. 1, Wiley and Sons, New York, 1950.

[7] A.S. Grove, Physics and Technology of Semiconductor Devices, Wiley and Sons, New York 1967.

[8] R.G. Oswald, etal, "Application of Tape Chip Carrier Technology to Hybrid Microcircuits", Proceedings of the Hybrid Microcircuit Symposium, June 8-9, 1976, U.S. Army Electronics Command, Ft. Monmouth, N.J.

[9] T. Angelucci, " Gang Lead Bonding Integrated Circuits", Solid State Technology, July 1976.

[10] J. Lyman, "Special Report: Film Carriers Star in High-Volume IC Production, Electronics, Dec. 25, 1975.

[11] G. DeHaine, etal, "Tape Automated Bonding Moving into Production", Solid State Technology, Oct. 1975.

APPENDIX A

AUTHOR	SUBJECT	TIS NO.
GK Baxter JW Brouillette	Heat Transfer	R75ELS027 DATE MAY 1975
TITLE THERMAL RESISTANCE OF MICROELECTRONIC PACKAGES		GE CLASS 1 GVT CLASS none
REPRODUCIBLE COPY FILED AT TECHNICAL INFORMATION CENTER ELECTRONICS LABORATORY SYRACUSE, N.Y.		NO. OF PAGES 63

SUMMARY

Methods for measurement of thermal resistance and temperature response curves, including MIL-STD-883 Method 1012, were evaluated to determine an optimum method to measure MIL-M-38510 packages.

Computer simulations, infrared measurements and electrical temperature sensitive parameter measurements of special thermal test packages were evaluated and compared. A ratio of about 5:1 was shown to exist for temperature rise values of the junction peak temperature, junction average temperature and the junction region temperature. Measurements can be very misleading unless precautions are taken to interpret results properly.

The optimum method, IR measurement of a coated chip, can only measure the temperature of the junction region.

KEY WORDS Integrated Circuits, Junction Temperature, Computer Simulation, Experimental Testing, Test Methods, Thermal Resistance, Infrared Temperature Measurement, Temperature Sensitive Electrical Parameters, Thermal Time Constant, Temperature Response, Thermal Models, Experimental Data, MIL-M-38510 Packages, Microelectronic Packages.

INFORMATION PREPARED FOR USAF/Rome Air Development Center (RBRM), Griffiss AFB, Rome, NY 13441

WORK CONDUCTED BY Authors

APPROVED B J Waterhouse, SS MGR D E Haas, SECT MGR

APPENDIX B

AUTHOR	SUBJECT	TIS NO.
G.K. Baxter	Test Methods and Procedures	R75EL8026
		DATE MAY 1975
TITLE A NEW RECOMMENDED METHOD 1012 (THERMAL CHARACTERISTICS) FOR MIL-STD-883		GE CLASS 1
		GVT CLASS None
REPRODUCIBLE COPY FILED AT TECHNICAL INFORMATION EP 13	ELECTRONICS LABORATORY SYRACUSE, N.Y.	NO. OF PAGES

SUMMARY

This new method specifies test procedures, measurement locations and descriptive notations for measuring and specifying junction peak temperature, junction average temperature and junction region temperature, chip carrier temperature, relative thermal time constants and relative thermal resistance values for microelectronic packages.

These methods will enable a user to make direct comparisons between thermal data provided by different vendors; and moreover, the data provide a meaningful interface for integrating vendor's data into the thermal design of the user's electronic system.

It is anticipated that a new industrial standard will evolve from the techniques and notations recommended during this study.

KEY WORDS Integrated Circuits, Junction Temperature, Experimental Testing, Test Methods, Thermal Resistance, Infrared Temperature Measurement, Temperature Sensitive Electrical Parameters, Thermal Time Constant, Temperature Response, Microelectronic Packages, Transistors, Diodes

INFORMATION PREPARED FOR USAF/Rome Air Development Center (RBRM), Griffiss AFB, Rome, NY 13441 AF Contract No. F30602-74-C-0150, Project No. N 4 E601.

WORK CONDUCTED BY Author (Project No. E-LAB. 263-DZ-804200)

APPROVED B J Walker
SS MGR

SECT MGR

APPENDIX C

ANALYSIS OF INFRARED MEASUREMENT TECHNIQUES

There are several possible problems associated with IR measurements on a semiconductor chip that are discussed below. This information came up during the process of evaluating the IR measurement technique and is thought to be of sufficient value to be included in this final report. The actual tests performed in determination of the optimum IR measurement technique are described in more detail in Appendices A and B. If we start at the surface of a typical chip and survey the problems we can encounter we will find contributions from the following effects.

OVERGLASSING

First, the overglassing, since it is the first layer of material on the chip and its IR transmission properties can be related to other facets of IR measurement similar to these described. An overglassing material, such as silicon oxide or silicon nitride is generally deposited to a thickness of about 0.5 μm on the chip surface to act as a protective layer. Silicon oxide, for example, is deposited in an oxygen lean atmosphere which results in a material somewhere between SiO and SiO_2; in some applications a little phosphorous may be added.* The problem this overglassing material may present depends on its thickness and its IR transmittance across the wavelength range of interest, i.e. that range for which the IR detector is sensitive. For example the transmittance of a 1mm thick silica glass falls from about 90% to about 10% across the band 2-5 μm.† Presumably, the transmittance of SiO_X is similar to that of the silica glass, SiO_2. Consequently, it is possible that the detected longer wavelength radiation may originate at the surface of a piece of glass while the shorter wavelength radiation may originate below the glass. This effect may become important for some overglassing materials and also in the case where a glass slide or other material is used to cover the cavity over an exposed semiconductor chip during IR measurements of microelectronic packages.

---

* Conversations with Dr. David D. Meyer, General Electric Company, Solid State Applications Operation, Integrated Circuit Center Devices and Processes, Syracuse, New York.

† Reference [2], Section 11, p. 16.

In tests during this project we were interested in the IR range of 1.8-5.5μm but the thinness of the silicon oxide overglassing on the thermal test chip negated any problem. The transmittance is equal to $\exp(\alpha_\lambda t)$ where t is thickness and α_λ is a wavelength dependent absorption coefficient per unit of thickness. For our 0.5μm thickness it is estimated that more than 99% of the energy is transmitted through the overglassing even at the longer wavelength.

METALLIZATION

Now to the second layer of material. If the second layer of material happens to be metallization then we encounter a real problem for infrared measurements. Most metallization films, such as the aluminum metallization of interest here, has an extremely high reflectance of nearly 100% in the IR range of interest. Since emissivity is equal to 100% less the reflectance, then the emissivity is obviously very low. For example a freshly evaporated film of aluminum has a reflectance of about 95% between 2-5 μm, hence the emissivity is only about 5%.* Consequently, radiation from the metallization is very low and therefore hard to detect and provide accurate measurement and conversion to equivalent temperature. An infrared microscope detects energy from an area centered at the crosshair location. If the metallization happens to fall within that area the metallized surface may not contribute a significant amount of energy to the total radiance measured by the detector; hence, the indicated temperature measurement may be very low.

SILICON CHIP

The second layer material that will generally be encountered, next to the metallization, is most probably the silicon chip itself, which has its own unique infrared transmission characteristics. Silicon is fairly transparent to infrared energy in the 2-5 μm wavelength range. A thickness of 2.54 mm has a transmission of about 55% in this range.* For a thickness of about 300μm (12 mils), similar to that for a typical semiconductor chip, the transmission increases to about 93%. Thus, energy radiating from a chip comes partially from the silicon material itself but primarily from the material layers below the chip. That material will usually consist of either the chip to substrate bonding material or the chip carrier (or substrate metallization) depending on the package construction and voids etc. in the chip bond.

Here again, we most probably will meet the low emissivity problem associated with metallization; consequently, it can be presumed that of the energy radiated from the chip, the largest portion may actually be reflected energy from the chip bond interface and the rest emanates from within the bulk material of the chip. A visual analogy to this might be that of looking from an airplane into the fairly clear water of a quiet shallow bay wherein the bottom of the bay has an almost mirror-like finish. What we attempt to see or detect in the bay is the surface condition of the water. That is very difficult. So it is with an infrared microscope, it is focused on and attempts

* Reference [2], Section 11, page 242, 243.

to detect or see the surface radiation from the chip. In reality it is detecting energy emanating from within the chip and reflected from the metallization, or radiated from the substrate, below the chip.

CHIP COATING

The best way to eliminate the chip translucence problem is to provide a coating on the surface of the chip. This in itself presents other problems however because a temperature gradient will occur in any coating. That means a lower surface temperature will be read because the surface is farther away from the junction and, in addition, the coating may alter the heat flow paths from the junction, resulting in an actual decrease of the junction temperature. Ideally then, the coating should be as thin as possible yet opaque in the IR wavelength range of the detector and should have a very high thermal resistance to lateral heat flow.

During experimentation with various inks, lacquers and enamels using different colors and solvents and methods of application such as spraying, daubing and spinning it became apparent that the best immediate coating solution would use some kind of a pigmented lacquer with very fine pigment particles. The size of these particles is very important because a uniform emissivity is desired over the whole detection area regardless of how small the area is in practice. The emissivity of a pigmented lacquer increases with thickness and a minimum practical thickness turns out to be about 25 μm (1 mil). At this thickness the emissivity in the infrared and visible regions is about 90% and 20%, respectively, for white pigmented lacquer on aluminum foil and about 95% and 95%, respectively, for black pigmented lacquer on aluminum foil.* Since the uniformity of the coating must be detected visually, it becomes important that the emissivity, or in reality -- the reflectivity, in the visual range, 0.4-0.7 μm, give sufficient contrast between the coating and the chip surface to detect nonuniform coatings. Consistent IR measurements can only be obtained with this relative thin coating if it is uniform in thickness. As it turns out, black pigmented lacquer gives much better visual contrast than does the white pigmented lacquer and is therefore recommended for the coating material.

REFERENCES

[2] J.A. Mauro, Optical Engineering Handbook, © 1966, General Electric Company, Electronics Laboratory, Syracuse, New York.

APPENDIX D

AUTHOR	SUBJECT	TIS NO.
R. McCarthy J.W.Brouillette	020 Reliability 040 Measurements	R76ELS025 DATE Aug. 1976
TITLE Improved IR Surface Temperature Measurements for Integrated Circuits		GE CLASS 1 GVT CLASS none
REPRODUCIBLE COPY FILED AT TECHNICAL INFORMATION EP 3	ELECTRONICS LABORATORY SYRACUSE, N.Y.	NO. OF PAGES 12

SUMMARY

Reliability predictions for integrated circuits would be improved if accurate IR surface temperature measurements were available. There are two methods presently in use, neither of which is satisfactory. The first method uses no surface coating, in which case the temperature measurements are inaccurate due to the changing emissivity across the surface. The second method uses a coating to produce a constant emissivity across the surface but, since, the coating is opaque to visible light, it is difficult to locate the measurement sites. Consequently, a search was performed to find a coating that is both highly absorbent in the IR (to produce a constant IR emissivity across the surface), and transparent in the visible spectrum (allowing the location of measurement sites). Two potential candidate coatings were found.

KEY WORDS

Integrated Circuits, coatings, IR measurements emissivity, reliability

INFORMATION PREPARED FOR NSF

WORK CONDUCTED BY Author

APPROVED _____ _____

SS MGR SECT MGR

TABLE OF CONTENTS

I. STATEMENT OF THE PROBLEM

To determine the performance and useful life of an integrated circuit in high reliability applications, accurate junction temperature measurements are needed. The devices within the integrated circuit exhibit wide variations in infrared transmissivity and emissivity, making it difficult to obtain accurate temperature measurements. Therefore the integrated circuit must be coated with a material that produces a constant high IR emissivity and, at the same time, is transparent enough in the visible spectrum so that the smallest surface detail of the integrated circuit can be accurately located. The coating must also be thin enough to produce negligible thermal distortions.

The purpose of this study was to find a suitable coating material.

II. SPECIFICATIONS

The following materials guidelines were followed:

1. Absorption

   The coating should be absorbing in the infrared, especially within the spectral range of the detector from 1.8 to 5.5 microns.

2. Emissivity

   The emissivity should be constant and high across the surface of the coated integrated circuit; reference 1, page 14 states $E \geq 0.8$. In reading with the infrared microscope this means that a coating over light areas should read the same as a coating over dark areas so that the reading, as a coated circuit is scanned, remains the same. This ratio must not change as a function of temperature as stated in reference 1, page 14.

3. Thickness

   As per reference 1, page 14, the thickness should be between 25-50 microns.

4. Applied Area

   As per reference 2, page 2, the circular area should be 1.0 mm^2.

5. Proportionality to Standard Blackbody Curve

   The IR microscope readings should be as high, or almost as high, as for a blackbody as a function of temperature. Ideally, a plot of the IR microscope (mV) response versus temperature (^{o}C) should display the same curvature as the blackbody or be strictly proportional to the blackbody curve.

6. Applicability

The material should be easy to apply to the surface of the integrated circuit.

7. Corrosiveness

The material should be classified as non-corrosive.

8. Toxicity

The material should be classified as non-toxic.

9. Availability

The material should be readily available.

10. Temperature

The material should be stable from 60°C to 200°C to cover the entire range of operational IC parameters. Preferably the material should have a melting point above 200°C.

11. Preparation

The material should be easy to prepare and apply.

12. Thermal Conductivity

The thermal conductivity of the material should be low as specified in reference 1, page 14.

III. APPROACH

A. Specification Tests

The purpose of the specification tests is to verify conformance with specifications 1, 2 and 5, listed above. There are two tests, as follows:

Test I. This test yields the difference in reading between coated light and dark areas. A white substrate was placed on a heated thermocouple-monitored copper plate. A black dot of India ink was painted on the substrate and a coating was spun over the dot and white substrate. A heat sink compound was placed between the white substrate and the copper plate. (See Figure 1.)

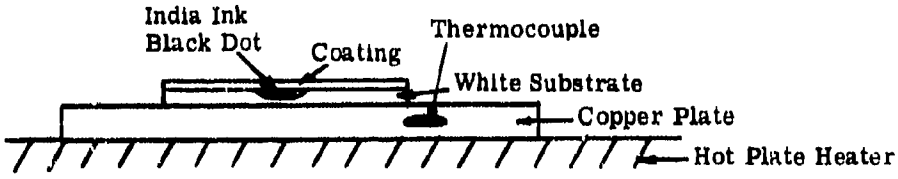


Figure 1. Emissivity Test.

The copper plate was heated to a specific operating temperature and the voltage output from the Barnes Infrared Microscope was recorded for the black dot and the white area. For a high emissivity controlled surface there should be little difference in readings.

The thickness of the layer was measured with a microscope.

The emissivity can be calculated as the ratio of the white to black area readings. Therefore, for high emissivities, $E \rightarrow 1$, the detector response reading between the white and dark areas would be approximately the same.

Test II. This test measured the voltage output of the IR microscope as a function of temperature, from 60°C to 200°C, for particularly promising coatings (from Test I). A plot of voltage versus temperature was obtained and compared with the same curve for the blackbody source.

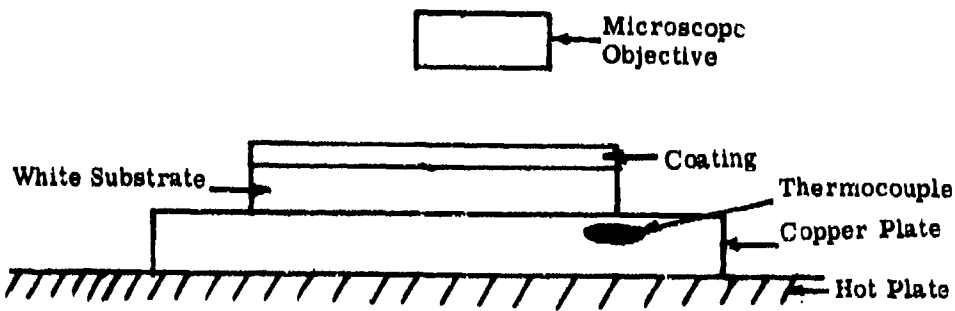


Figure 2. Temperature Response Test

A thin coating was spun onto a white substrate. The thickness of the coating was measured with a microscope. Then the substrate was placed on the copper plate and the temperature was varied from 60°C to 200°C. The output of the infrared microscope was recorded (see Figure 2).

B. Materials

The following materials were tested:

1. Versamids #900, #930, #940, #950
2. Lacquers
   Black Krylon, Clear, Matt Finish
3. Wratten Filters
   #52, #54, #48, #93, #102
4. Carbon Evaporation
5. Glycerin

6. Sodium Silicate

7. Versamid Mixtures
   with Versamids, with glass.

8. Glycerin Mixtures
   Glycerin and glass

9. Sodium Silicate Mixtures
   Sodium Silicate and glass

Each of the materials tested had absorption regions in the IR as measured by the IR Spectrum Analyzer (see Figure 3). Emissivity and absorption data for these materials are presented in Table I.

IV. RESULTS

A. Instrumentation

The spectral response of the Barnes IR microscope is shown in Figure 4. The Microscope was evaluated as follows:

1. Operator Instrument Variance

   After repeated testing, and neglecting the constant instrument variance in the microvolt range, there is an operator instrument variance of 0.6 mV average, which renders the last three digits of each reading highly inaccurate. For example, a reading of 0.023456 appears as

   0 . 0 2 3 4 5 6

   Operator/Inst. Variance Random Changes ,

   which means that the reading is 23 mV ± .6.

2. Mechanical Variance

   As the microscope is operated in and out of focus with the high power objective, it does not always return to the original target area. This may be one of the reasons for the Instrument/Operator Variance noted above.

3. Temperature Response

   There is a difference in readings when increasing or decreasing temperature, which averages out to approximately 1 mV. Readings should always be taken as the temperature is increasing since the deviation is rather large compared to other variances.

TABLE I. EMISSIVITY AND ABSORPTION DATA

	Emissivity = White Area Reading / Black Area Reading	Absorption Compared to Blackbody at 70°C Blackbody was 75.00 mV
Evaporated Thin Coat-Carbon	0.46	
Ver. 900 (200 microns)	0.58	40.82
Clear Lacquer	0.57	33.90
Ver. 950	0.59	50.60
Mix 50:50 Ver. 930+940	0.74	71.92
Mix 50:50 Ver. 940+950	0.55	69.00
Mix 50:50 Ver. 930+950	0.83	48.66
Mix 50:50 Ver. 900+930	0.75	55.09
Mix 50:50 Ver. 900+940	0.77	73.00
Mix 50:50 Ver. 900+950	0.86	62.50
Mix 75:25 Ver. 950, 920	0.75	55.23
Mix .33, .33, .33 Ver. 900, 940, 950	0.66	65.52
Ver. 900 + Crystal Glass	0.91	73.40
Glycerin	0.71	no data taken (see chart)
Glycerin + Glass	0.99	
Sodium Silicate	0.795	no data taken (see chart)
Sod. Sil. + Glass	0.99	

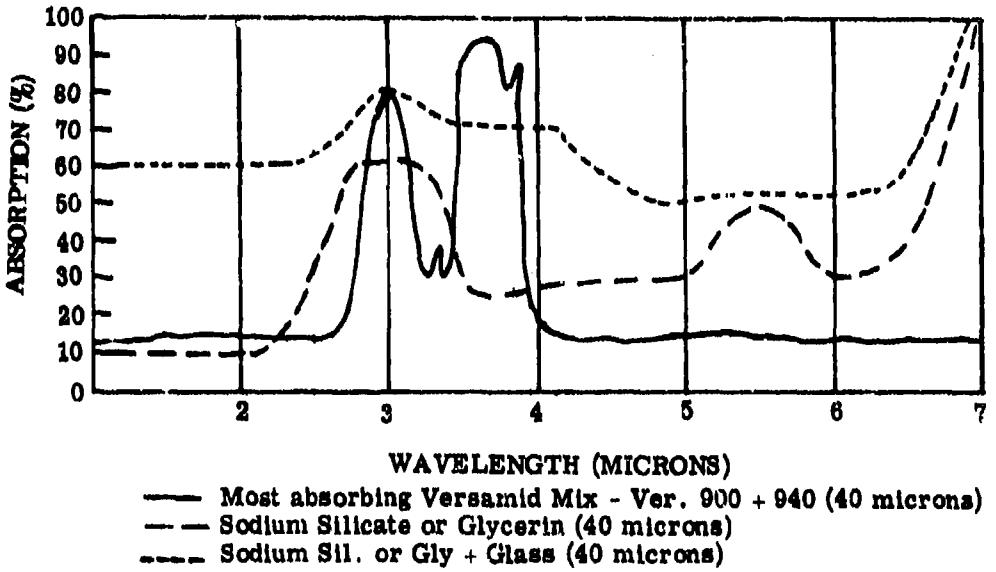


Figure 3. IR Spectrum Analysis Curves.

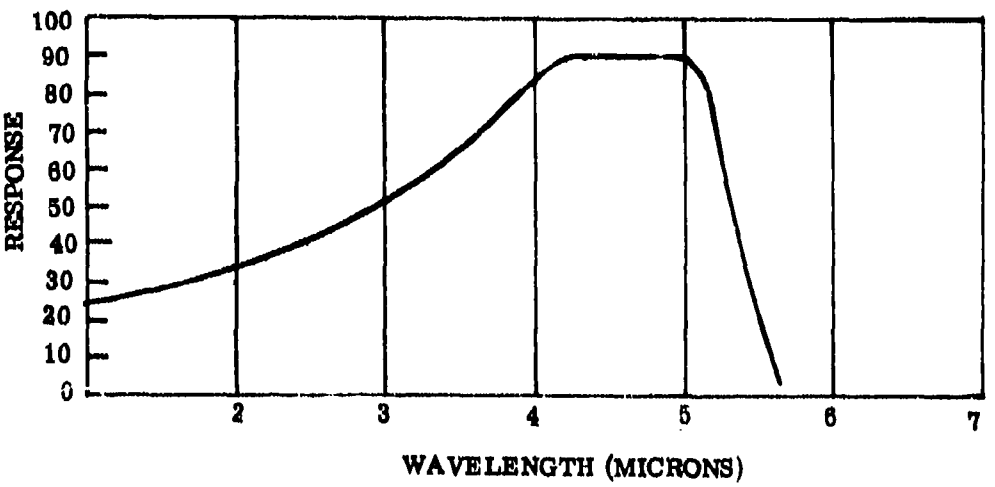


Figure 4. Spectral Response of Barnes IR Detector.

4. Temperature Differentials

It was noted that when the objective was placed near the specimen the temperature recorded by the thermocouple decreased. Also, when blocking off the objective the detector monitor no longer recorded near zero, but now indicated a reading of approximately 0.00500 or 5 mV. This reading, probably due to the heated objective, stayed fairly constant, even when the temperature of the hot plate was increased. Because of the discrepancy in returning to the same spot, due to mechanical tolerance, it was decided to leave the microscope in place, increase the temperature, and take detector output readings without recalibrating after each temperature reading.

5. Optical Constraints

Using the high power objective it was impossible to focus on the surfaces of the IC with the package used in the tests; therefore the low-power objective was used. In order to get near enough to the IC to focus the high-power objective, it must be redesigned, or a slightly larger focal length must be used.

6. Blackbody Calibration

The blackbody calibration used as the standard for all tests is shown in Figure 5, Curve A.

B. Materials Testing

1. Versamids and Versamid Mixes

Thick layers of versamids were very absorbing in the IR region but, after spinning and obtaining a thin layer, most of their absorbance was lost. On heating, the layer became increasingly opaque with increasing temperature. This occurred in versamid mixes as well.

2. Wratten Filters

Wratten filters of gelatin were found to be unstable above 50°C and glass filters were too thick for this application.

3. Lacquers

On all lacquers tested, which were transparent in the visible, emissivity was not constant across the specimen and the IR absorption was not high.

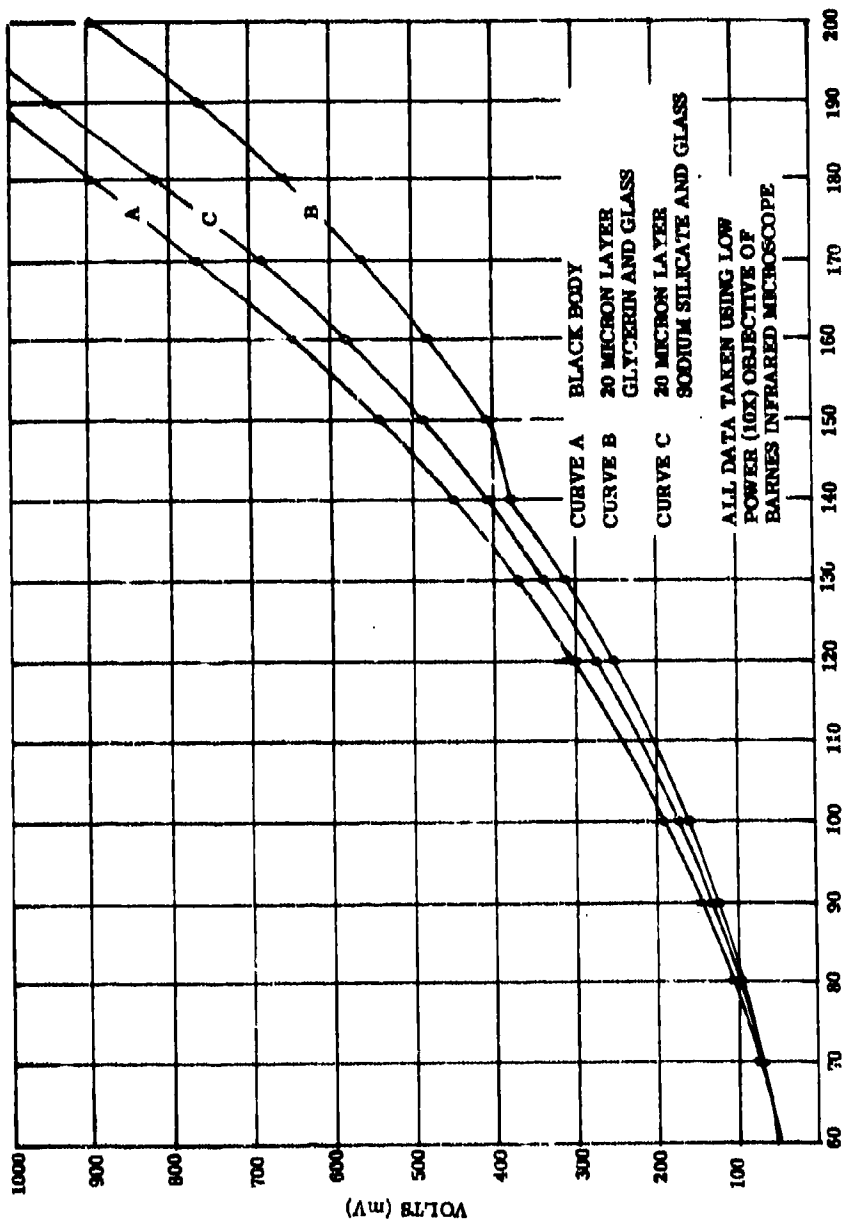


Figure 5. Detector Voltage as a Function of Temperature. (Complete Temperature Profile).

4. Carbon

In initial tests using an actual IC a thin layer of carbon was evaporated onto the IC. The emissivity was almost constant but the resolution was poor, especially in light of the fact that we used a relatively simple IC package with few components. This process would be suitable for this type of package but, for LSI or MSI applications, the resolution would be a problem.

5. Glycerin and Glycerin Mixes

A glycerin coating produced a large deviation when measured across the sample, especially for a thin layer. When fine particles of glass were added to the glycerin there was no difference when scanning across the sample. The best thickness of glass particles was about 60 microns, with particles ranging from 2 to 30 microns. Milling the glass to smaller sizes — (all below 20 microns) a thin layer of 20 microns was obtained. A plot of detector voltage vs. temperature for this layer is shown in Figure 5, Curve B. Complete evaporation took place between 140°C and 150°C. It should be noted that the readings decreased after complete evaporation. Different concentrations of glass had little effect on the results either in evaporation or in emissivity.

6. Sodium Silicate and Sodium Silicate Mixes

Sodium silicate coatings did not yield high emissivities, but a 50-50 mixture of silicate and glass did absorb highly in the IR range and exhibited a high emissivity. Also, the sodium silicate did not evaporate. The detector voltage versus temperature curve is shown in Figure 5, Curve C. The sodium silicate/glass mixture is a good coating material, provided it is not required that the coating be removed. It is extremely difficult to remove this coating once it has been heated above 70°C. Ultrasonic cleaning can be used to remove this coating but it may damage the IC, especially the fine wires attached to the circuit.

V. CONCLUSIONS

Black Krylon paint absorbs heat. The IR microscope focused on heated black Krylon paint shows a relatively high reading because the black paint absorbs and gives off IR energy in relatively large amounts. Glass also absorbs in the IR but, unlike the black paint, is transparent in the visible IR spectrum.

Even thin coats of glass will absorb and radiate almost as much IR as the black Krylon paint. Therefore the problem was to find a way to put a thin layer of glass on the integrated circuit so that the coating is as absorbing as the black paint.

It was found that when glass particles of about 10-15 microns are suspended in a homogeneous medium some of the specular radiation scatters and becomes diffuse, heating the coating to the approximate temperature of a blackbody. As long as the homogeneous medium is transparent the coating will be transparent, even though it appears that it absorbs in the IR as the black paint.

Sodium silicate is not a highly absorbing coating in the spectral range of the detector. Glass, however, is highly absorbing in this region while transparent in the visible. It was thought that, by using particles of glass suspended in a medium, the resulting coating would have a high absorption in the IR and the spectral range of the detector and, as long as the glass remained suspended in the medium, the IC component would be visible through the coating.

Any medium could probably be used, providing it was transparent in the visible, slightly absorbing in the spectral range of the detector, and would not evaporate at 200°C — the maximum operating temperature of the IC's to be tested. If the medium evaporates then the glass crystallizes on the surface of the IC and becomes opaque in the visible due to a change in the index of refraction. Its IR absorption also becomes somewhat less. This was the case with glycerin and glass above 140°C. Cooling the IC and adding more glycerin returns the coating to the original transparency that it exhibited in the visible. Sodium silicate does not completely evaporate until it reaches 1088°C and, therefore, a coating of glass and sodium silicate remains transparent in the visible throughout the temperature profile of the IC. It may flow somewhat or crack, but it does not allow the glass to fall on the surface. The index of refraction does not change with temperature. Also its proportional variance with the blackbody stays constant throughout the temperature profile, so that a correction can be applied to the reading when applying temperature calculations. Its form would be $X + AX$ where $A = 0.10$ and X would be the voltmeter reading for the coated IC at each temperature point.

The emissivity is constant across the IC throughout the temperature profile. However it may be desirable to use the fine-glass coating provided by the boil-off of glycerin and glass on the IC. Normally, the coating would be opaque, but when a drop of water or glycerin is placed on the coating, the index of refraction changes and it becomes transparent allowing one to locate components. The material selected (water or glycerin), depends on the operating temperature; that is, the materials rate of evaporation at the operating temperature. The material must evaporate at a rate slow enough for the operator to find the part of the circuit he wishes to test because, when total evaporation takes place, the circuit is no longer visible.

The method of preparation for glycerin and glass is the same as sodium silicate and glass (see section B below). This type of layer is much easier to remove from the IC than sodium silicate and glass, which may be an important feature for some applications.

Both of these coatings could be useful, and can be used to control surface emissivity. The choice depends on the application, parameters of the test, and operator preference. For higher temperatures, above 140°C, sodium silicate and glass are still more appropriate.

Testing the coating is prepared as follows:

1. Mount the IC to be coated on a spinner
2. Place a drop of sodium silicate (or glycerin) on a clean microscope slide
3. Stir into the sodium silicate (or glycerin) drop an equal amount of microscope slide glass, which has been previously crushed and milled to 20 μ or less.
4. Mix the sodium silicate (or glycerin) and glass thoroughly
5. Place the mixture quickly on the IC to be coated using a small wooden stick (the wooden part of a Q-Tip serves well). Gather the mixture on the end of the stick and lightly touch the IC with the coating on the end of the stick. Some of the mixture will adhere to the IC forming a drop on it.
6. Spin immediately at 2800 RPM (high 75 mark on dial) for 3 minutes.
7. Turn off the spinner and examine the IC to determine if layer is uniform. If not, immediately apply drops of boiling water to the IC to melt the coating away. The coating will run off the sides and it can then be spin-dried. Now, the IC is ready for another coating. Once the coating is uniform there will be, approximately, a 20μ coating on the IC and the IC is ready for testing.

References

1. Baxter, G.K., A New Recommended Method 1012 (Thermal Characteristics) for MIL-STD-883, General Electric, Technical Information Series, R75ELS026, May 1975.

2. Brouillette, W., Directory Copy - Faculty Research Participation, Improved Infrared Surface Temperature Measurements on Microelectronic Integrated Circuits, May 1976.